Protection for Field Transmitters: Requirements, Challenges, Solutions

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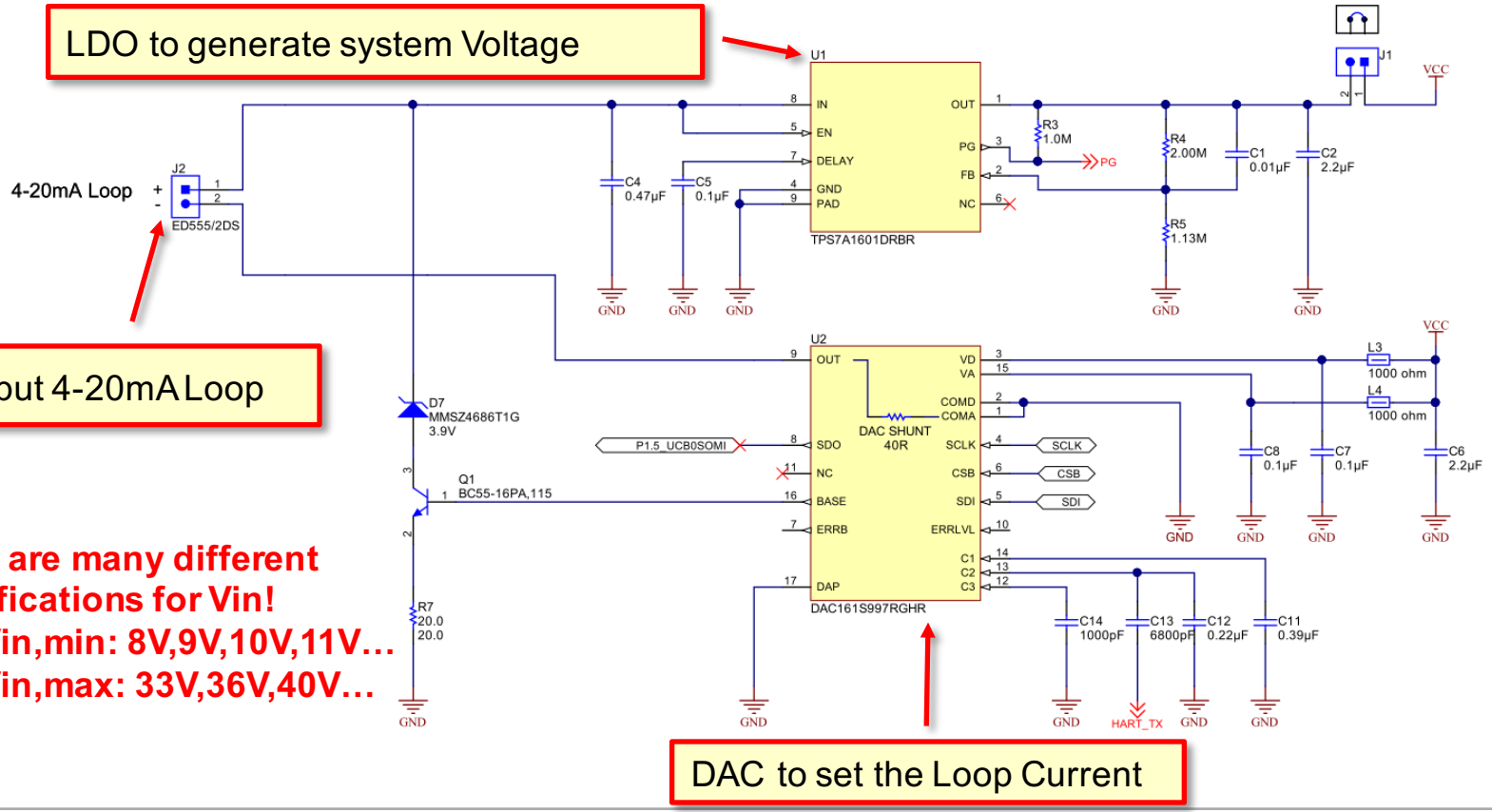
Agenda

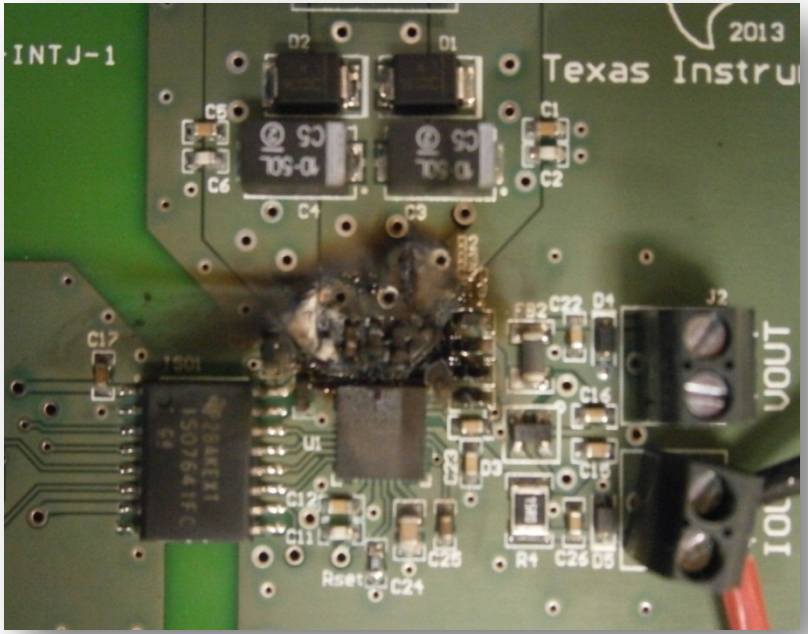
- Introduction to IEC61000-4 EMC Immunity Test Suite
- Surge Protection with TVS Diode and implications for the system
- Example Implementation 1: Loop-powered 4-20mA Transmitter
- Example implementation 2: Combined Voltage / Current output

Simplified circuit of loop powered 4-20mA Sensor



- **There are many different specifications for Vin!**
  - **Vin,min: 8V,9V,10V,11V…**
  - **Vin,max: 33V,36V,40V…**

Did you promote the correct solution…



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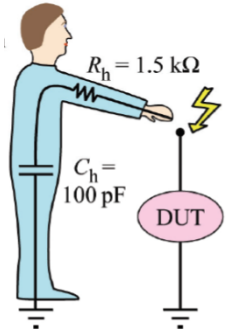
Catastrophic board failure during SURGE test

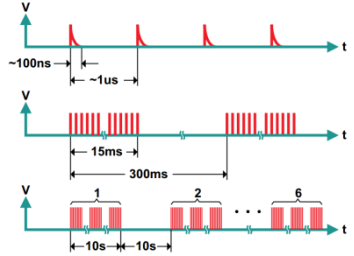
IEC61000-4 EMC Immunity Test Standards

IEC61000-4 contains 35 different immunity test standards

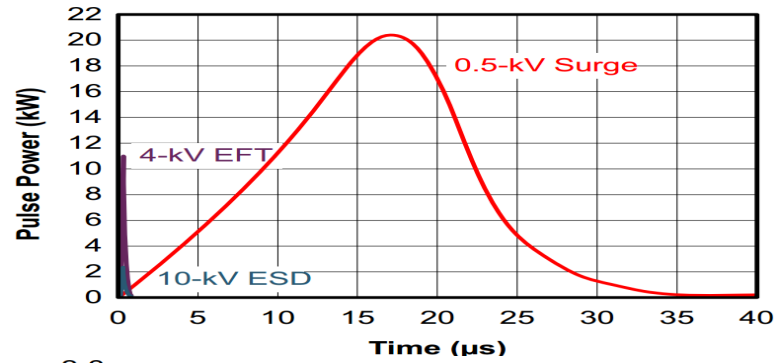


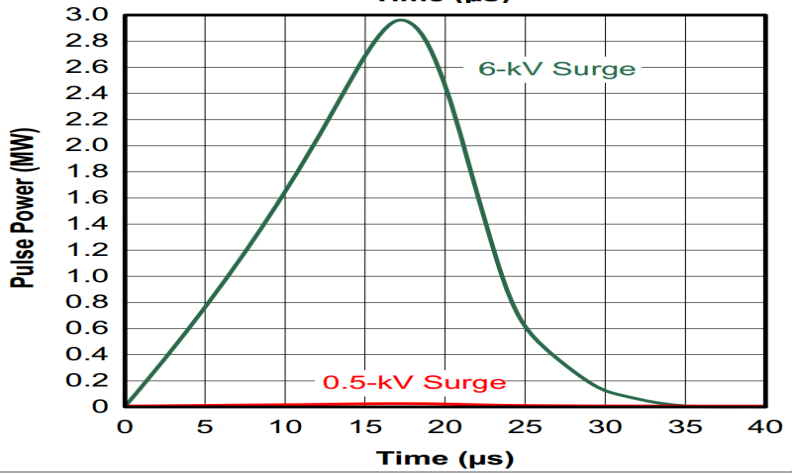
Most commonly applied immunity tests:

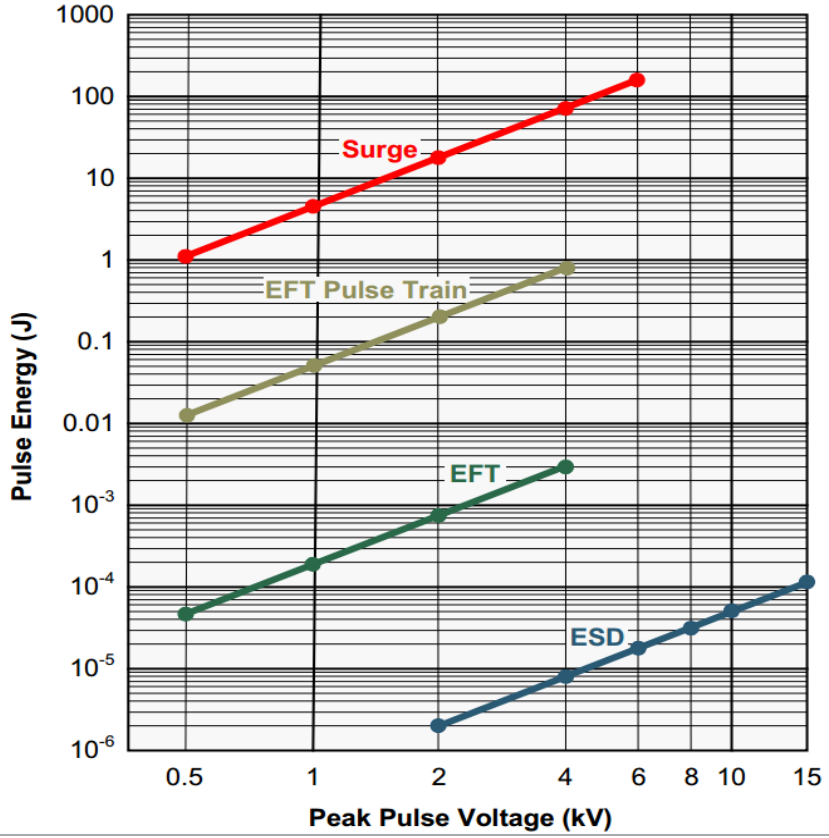
- Electrostatic Discharges
  - **IEC61000-4-2: Electrostatic Discharge Immunity**
- HF Conducted Disturbances
  - **IEC61000-4-4: Electrically Fast Transient Immunity**
  - **IEC61000-4-5: Surge Immunity**
  - IEC61000-4-6: Conducted Immunity Tests
- HF Radiated Disturbances
  - IEC61000-4-3: Radiated Immunity
  - IEC61000-4-9: Pulse Magnetic Field Tests
- LF Radiated Disturbances
  - IEC61000-4-8: Power Frequency Magnetic Field Immunity



Comparison of pulse power and pulse energy

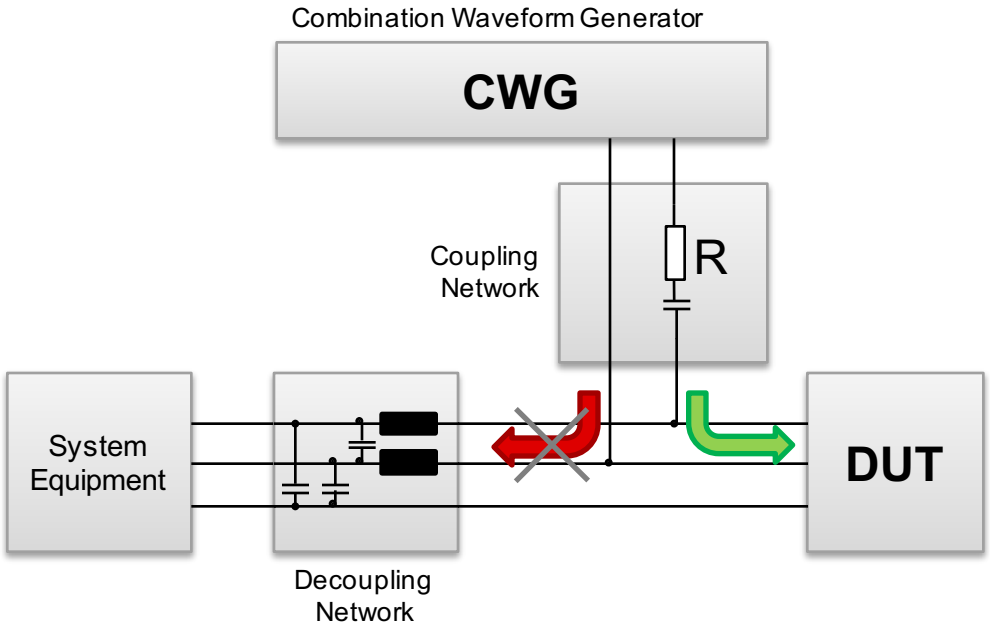


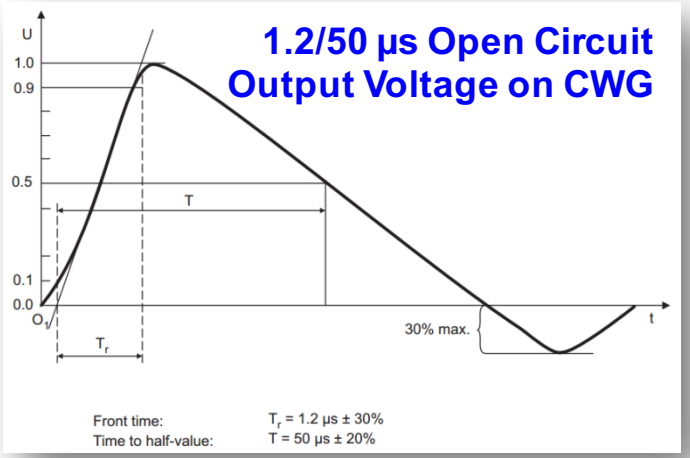


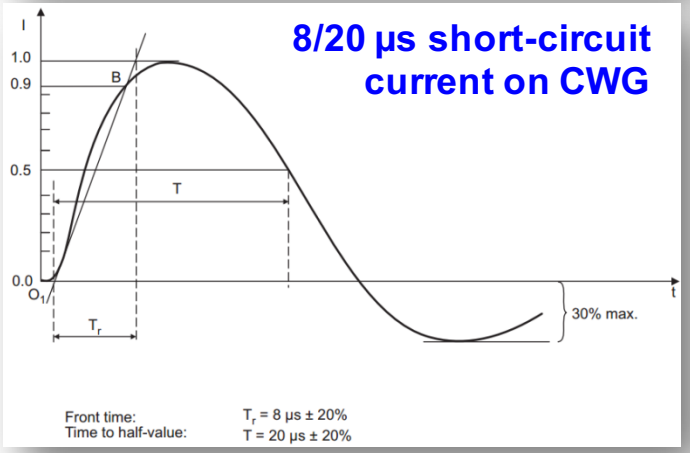


Source: Datasheet; SN65HVD7x 3.3-V Supply RS-485 With IEC ESD Protection; sllse11d

Example Test Setup







Source: App Report; IEC 61000-4-x Tests for TI's Protection Devices; slva711

EFT and Surge waveform equations and simulation models
https://e2e.ti.com/support/interface/industrial_interface/m/videos__files/665146/download

Voltage Levels, CN & Max Peak Currents

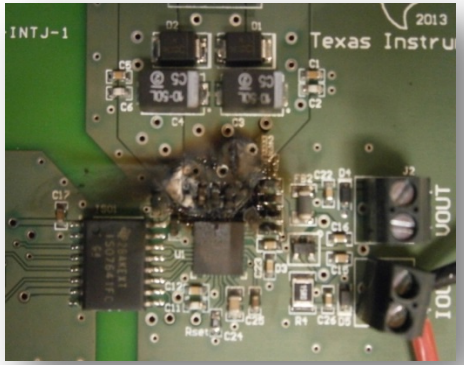
Level	Open Circuit Test Voltage [kV]	Description	Maximum Peak Current [A]		
			R=42Ω	R=12Ω	R=2Ω
1	0.5	Partly protected electrical environment	12	42	250
2	1	Electrical environment where the cables are well-separated, even at short runs	24	84	500
3	2	Electrical environment where cables run in parallel	48	167	1000
4	4	Electrical environment where the interconnections are run as outdoor cables along with power cables, and the cables are used for both electronic and electric circuits	96	334	2000
X	Custom	Special conditions specified in the product specification	x	x	x

- **Usually the dedicated product standard specifies the specific test conditions.**
- **Transmitter applications require most often to test with 1 kV / 42 Ω common mode, customers apply even differential mode**

Source: App Report; IEC 61000-4-x Tests for TI's Protection Devices; slva711

Performance Criteria for Surge (IEC 61000-4-5)

Performance Criteria	Description
A	Performance within specification limits
B	Temporary degradation which is self-recoverable
C	Temporary degradation which requires operator intervention
D	Loss of function which is not recoverable



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Which performance criteria is met?

How can the system be protected?

Examples:

- Transient Voltage Suppressor (TVS) Diode
- Gas Discharge Tube (GDT)
- Steering Diodes
- Current limiting circuitry
- Combination of the above mentioned

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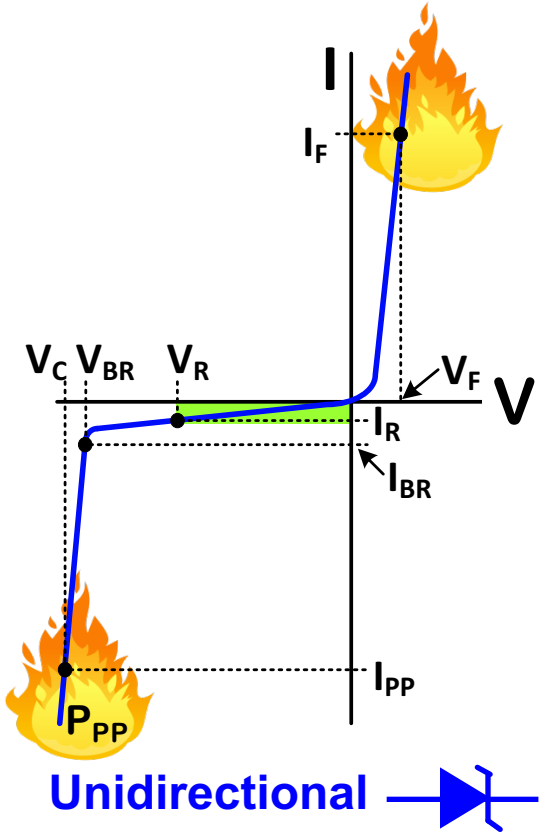
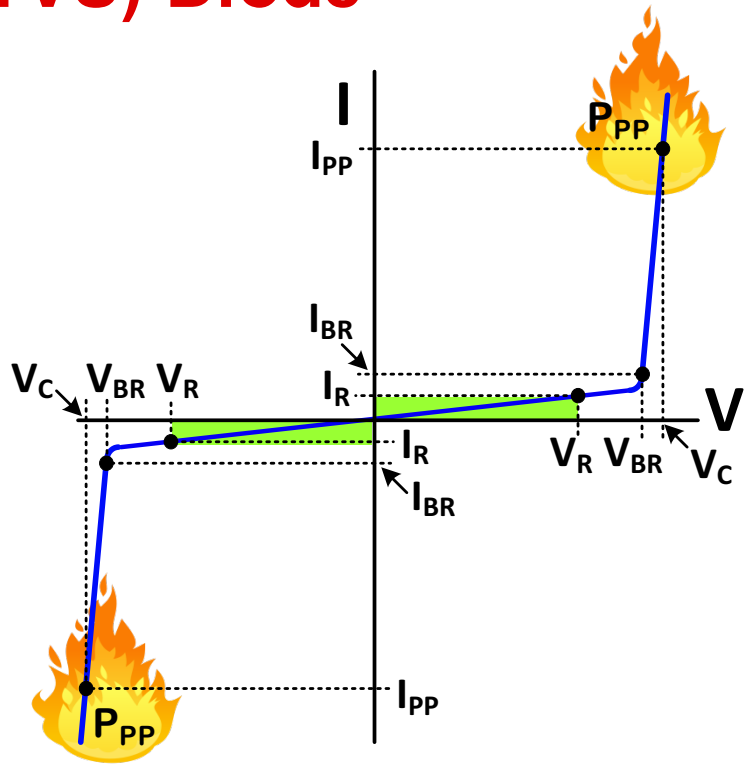
Transient Voltage Suppressor (TVS) Diode



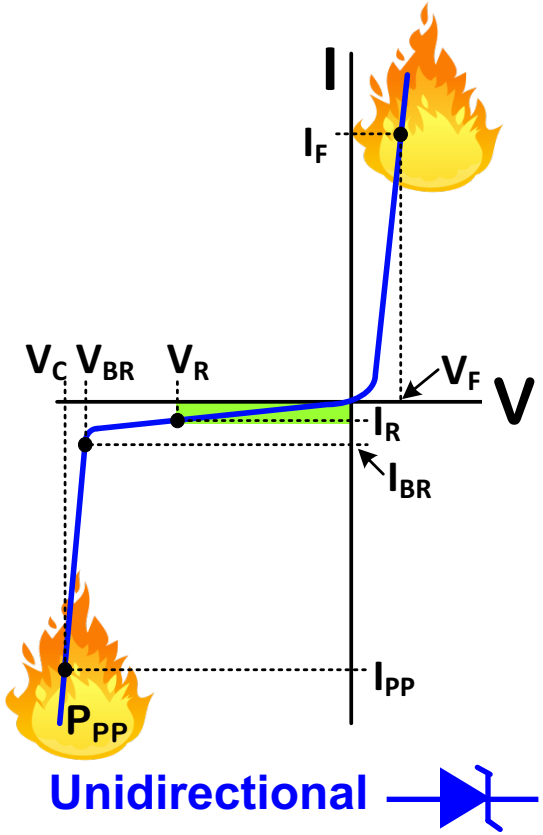
Unidirectional

Symbol	Parameter
V_R, V_{RM}	Stand-off voltage
I_R, I_{RM}	Reverse Leakage @ V_R
V_{BR}	Breakdown voltage @ I_{BR} & T
I_{BR}, I_T	Breakdown Current
αT	Temperature Coefficient of V_{BR}
V_C, V_{CL}	Clamping voltage @ I_{PP}
I_{PP}	Peak pulse current
R_D	Dynamic resistance
$P_{PP(M)}$	(Max) Peak pulse power
$V_{F(M)}$	(Peak) Forward voltage drop
$I_{F(M)}$	(Peak) Forward current



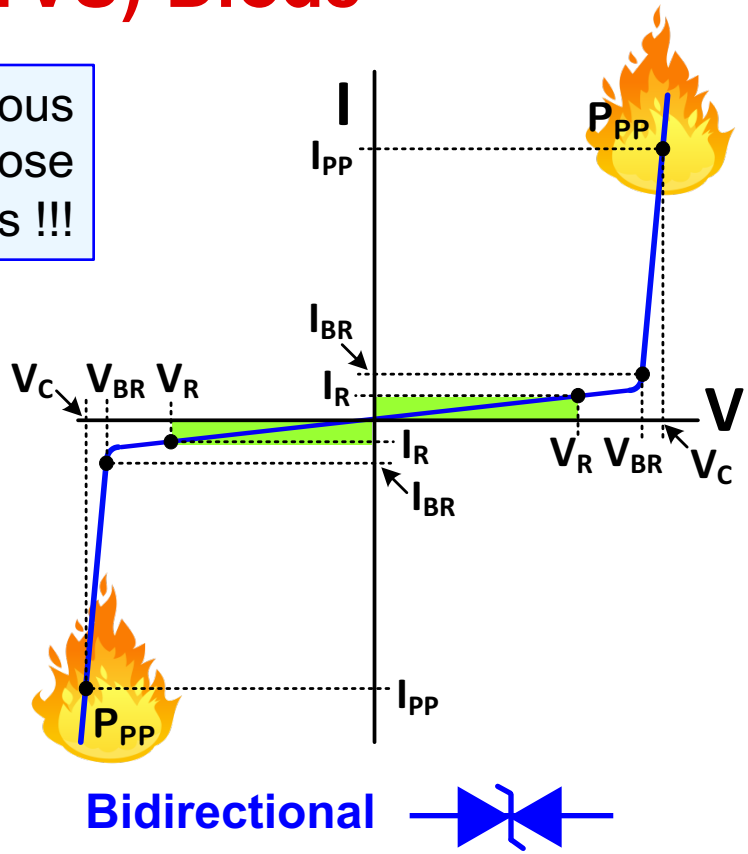
Bidirectional

Transient Voltage Suppressor (TVS) Diode



Unidirectional

No continuous operation at those conditions !!!



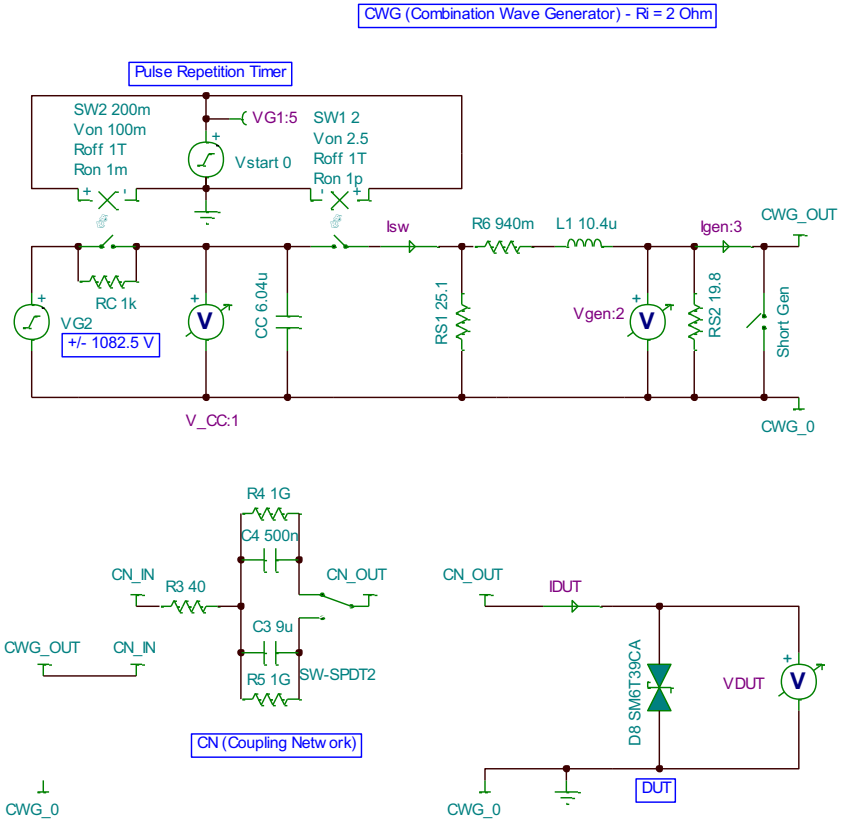
Bidirectional

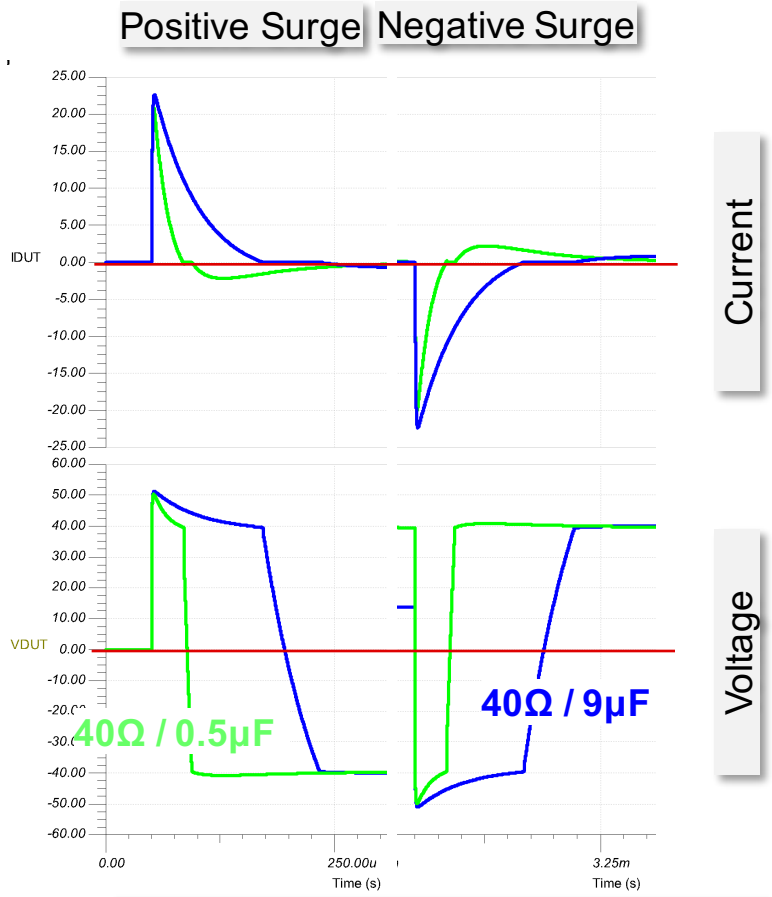
TVS – Standard series

	SMAJ	SMBJ	SMCJ	SMLJ SMDJ
Peak Pulse Power *	400W	600W	1500W	3000W
Package	 SMA DO-214AC	 SMB DO-214AA	 SMC DO-214AB	
Package Size	5.2 x 2.6 mm^2	5.4 x 3.6 mm^2	7.9 x 5.9 mm^2	
Package Area	13.52 mm^2	19.44 mm^2	46.61 mm^2	
Pad Size	5 x 5 mm^2			8 x 8 mm^2

* For 10/1000µs pulse

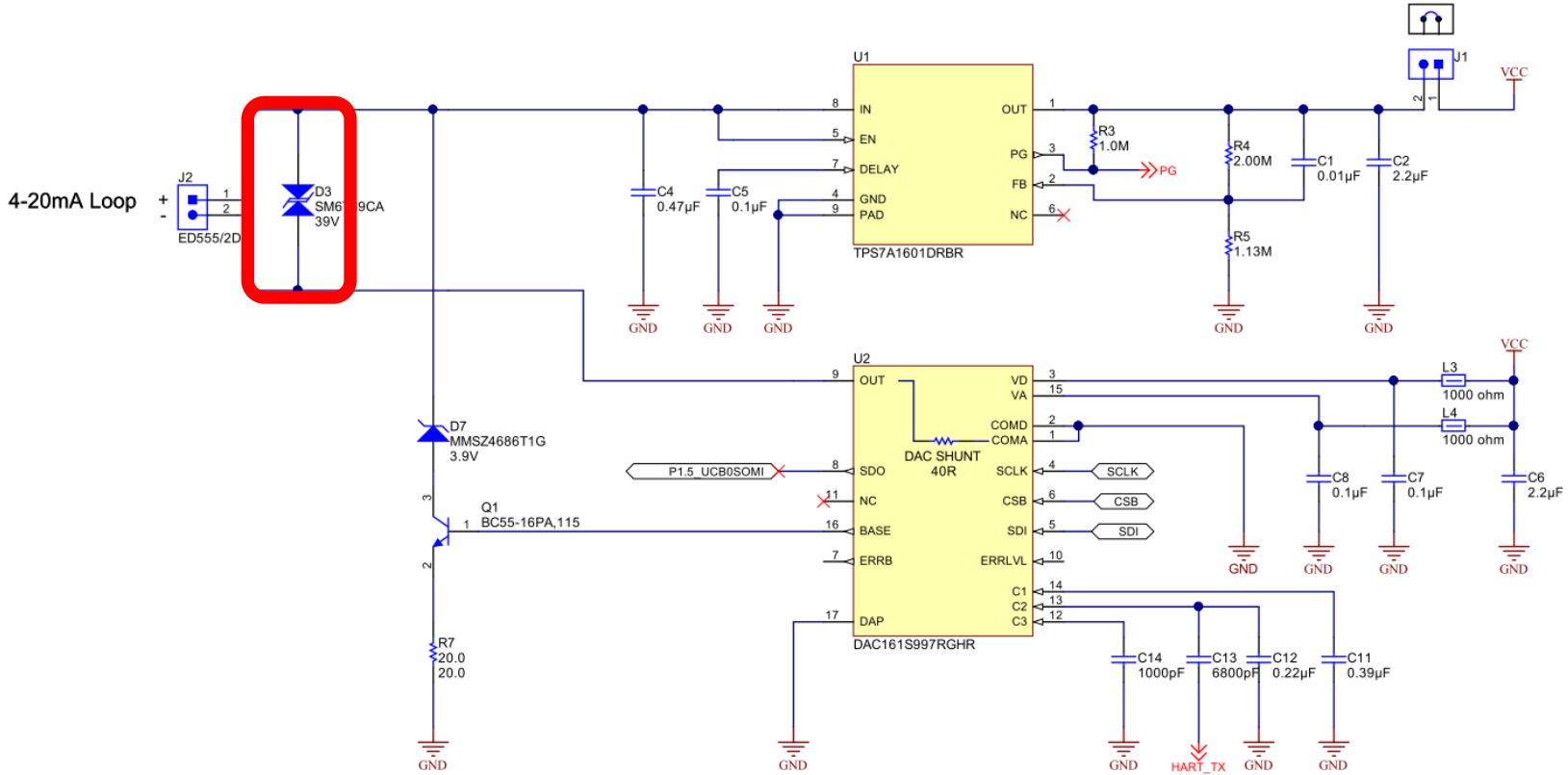
TVS - Basic Simulation





Any single surge current pulse leads to a positive / negative voltage pulse

Modified Schematic with TVS Diode at the Input



Example: TVS Diode Calculation

$P_{PP} = V_{CL} \times I_{PP} = 53.3V \times 11.3A = 602.3W$ @25°C; $10/1000\mu s$

Peak Pulse Power for 20µs from graph: 3.5kW **Not accurate**

From Temperature Derating graph (@125°C): 3.5kW ×70 % = 2.45kW

$$R_D = \frac{V_{CL} - V_{BR\max}}{I_{PP}} = \frac{53.3V - 40.6V}{11.3A} = 1.124\Omega$$

Only valid for 10/1000µs pulse

$V_{CL@25°C} = R_D \times I_{PP} + V_{BRmax} = 1.124\Omega \times 24A + 40.6V = 67.6V$

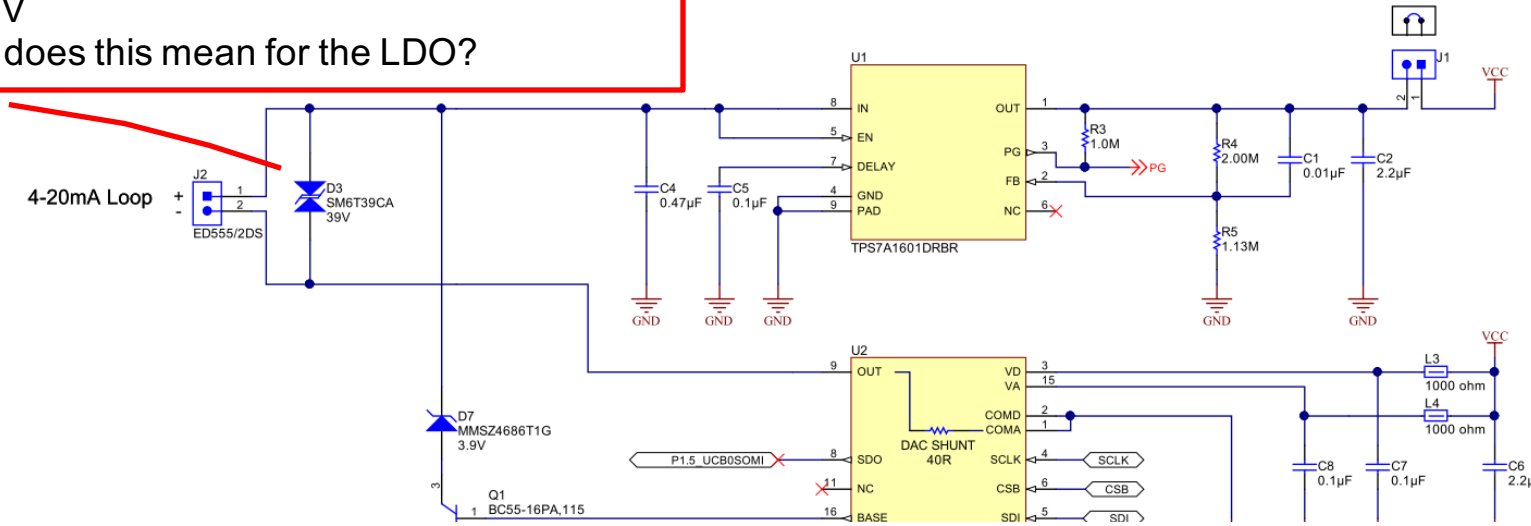
$P_{PP} = V_{CL} \times I_{PP} = 67.6V \times 24A = 1.62kW@25°C$ → **1.78kW@125°C**

$V_{CL@125°C} = V_{CL@25°C} \times \left(1 + \alpha T \times (T - 25)\right)$; αT=0.1%/°C (typical)

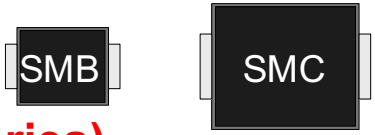
$V_{CL@125°C} = V_{CL@25°C} \times (1 + 0.001 \times 100) = 67.6V \times 1.1 = 74.36V$

Modified Schematic with TVS Diode at the Input

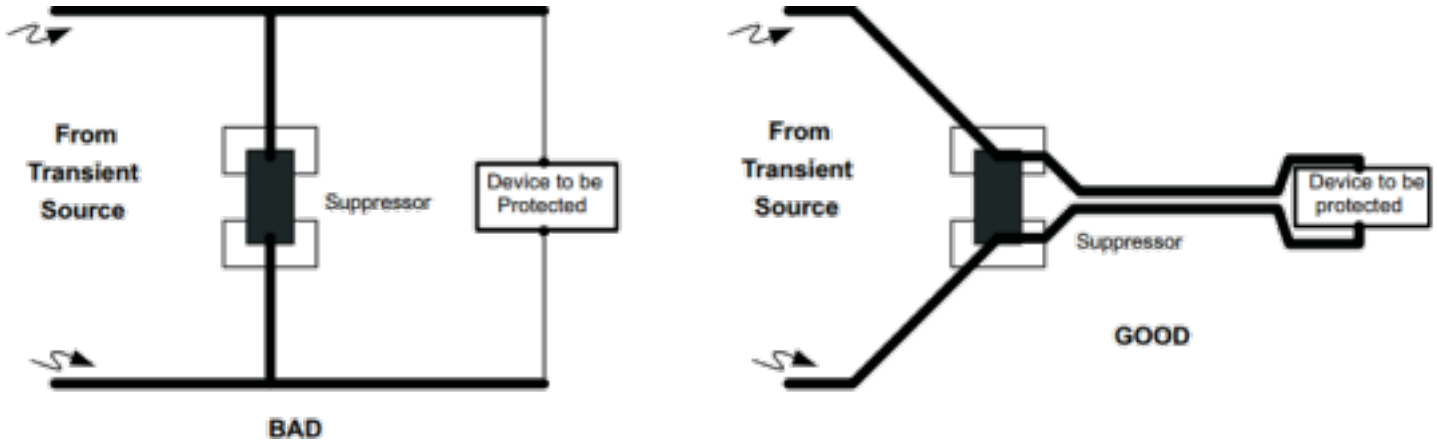
- 74.36V
- What does this mean for the LDO?



There is some uncertainty due to the different pulses.
Alternative: SMCJ series
Vcl=58.63V @28.2A; 125C; 10/1000µs
→ Package size: 7.9 x 5.9 = 46.6mm² vs. 19.4mm² (of SMBJ series)



TVS – Layout recommendations



- **Use 4-terminal connection type to mitigate parasitic inductance effect**
- **Place TVS on same layer as DUT**
- **Increase solder pad size to reducing heating of TVS**

App Report; Electrical Transient Immunity
for Power-Over-Ethernet; slva233a

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- Surge Protection with TVS Diode and implications for the system
- Example Implementation 1: Loop-powered 4-20mA Transmitter
  - Surge Protection
  - Reverse Polarity Protection
  - Current Limiting

  Examples: TIDA-00167, TIDA-00648, TIDA-00165, TIDA-00189
- Example implementation 2: Combined Voltage / Current output

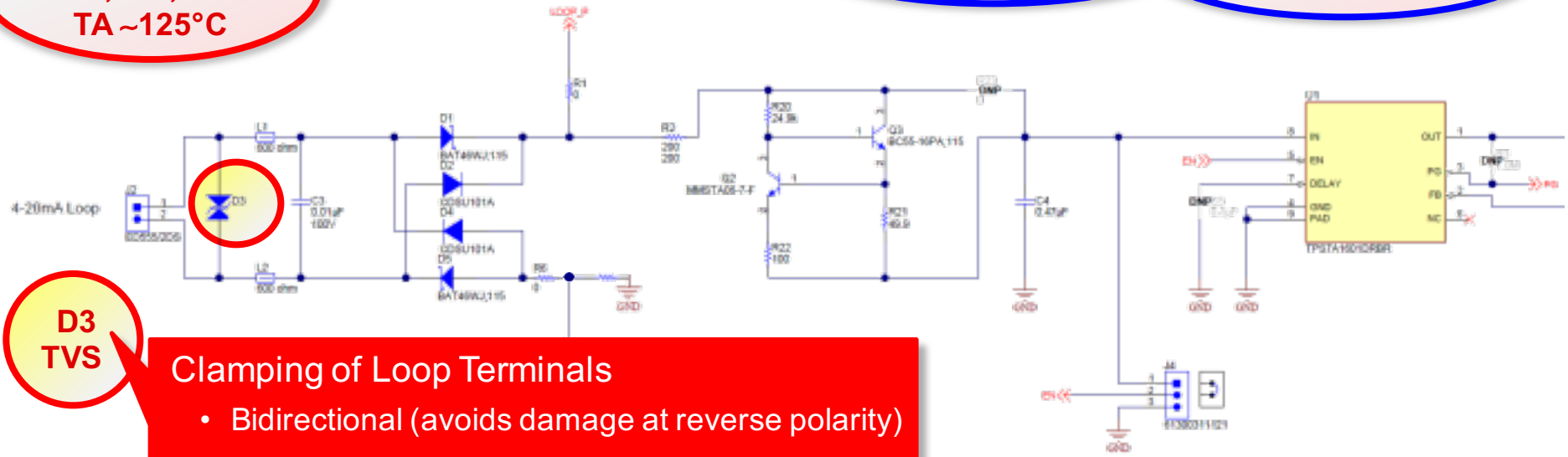
TVS usage – a real example

2-wire loop powered 4-20mA interface

Surge
1kV, DM, 42Ω
TA ~125°C

Q2 / Q3, NPN BJT
VCEO = 80 / 60V

U1, LDO
abs maxVIN=62V

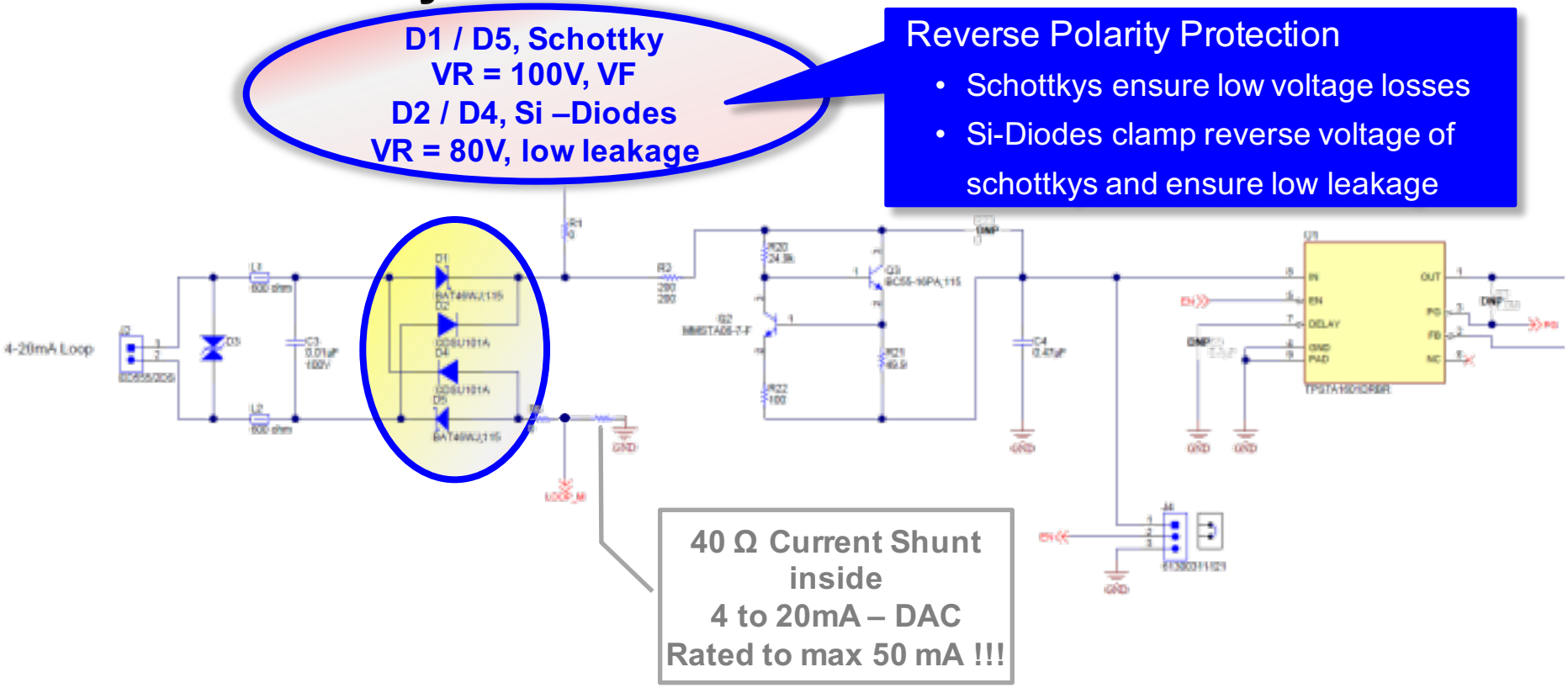


Clamping of Loop Terminals

- Bidirectional (avoids damage at reverse polarity)
- V_{CL_max} @ +125°C < $VIN_{max\_U1,\ Q2,\ Q3,\ C3,\ Dx,\ \ldots}$
- negligible leakage @ T_{max}, $VLOOP_{max\_nominal}$

2-wire loop powered 4-20mA interface

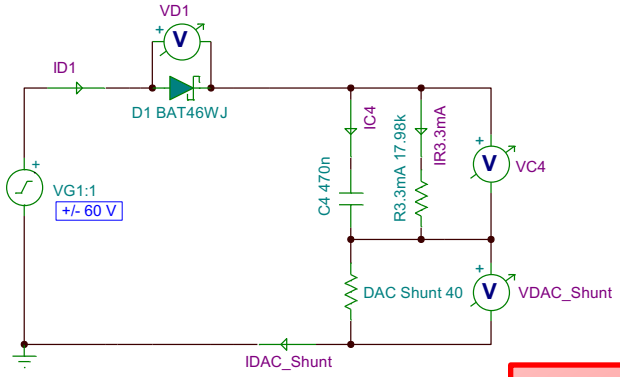
Reverse Polarity Protection

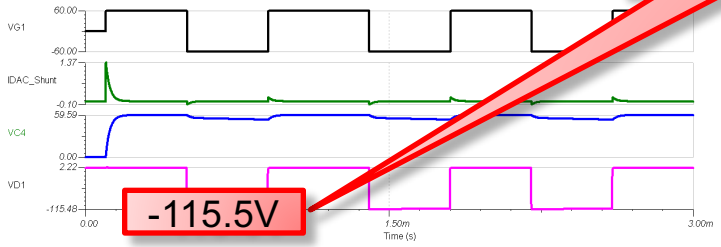


2-wire loop powered 4-20mA interface

Reverse Polarity Protection – Different Approaches (I)

Half-Wave Rectification (Single Diode)

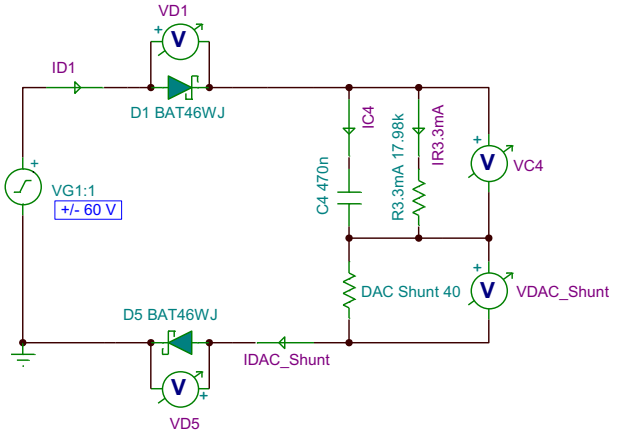




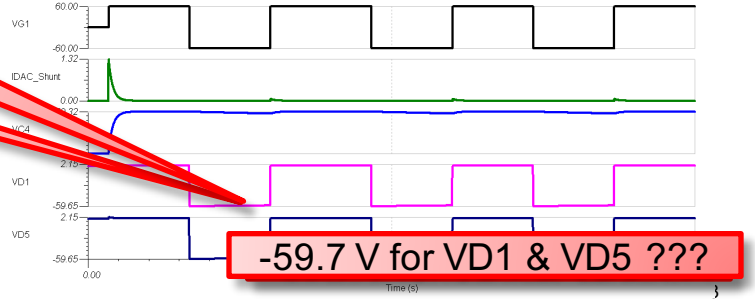
VR > 2 x VG

-115.5V

Half-Wave Rectification (Dual Diode)



VR > VG ???



-59.7 V for VD1 & VD5 ???

2-wire loop powered 4-20mA interface

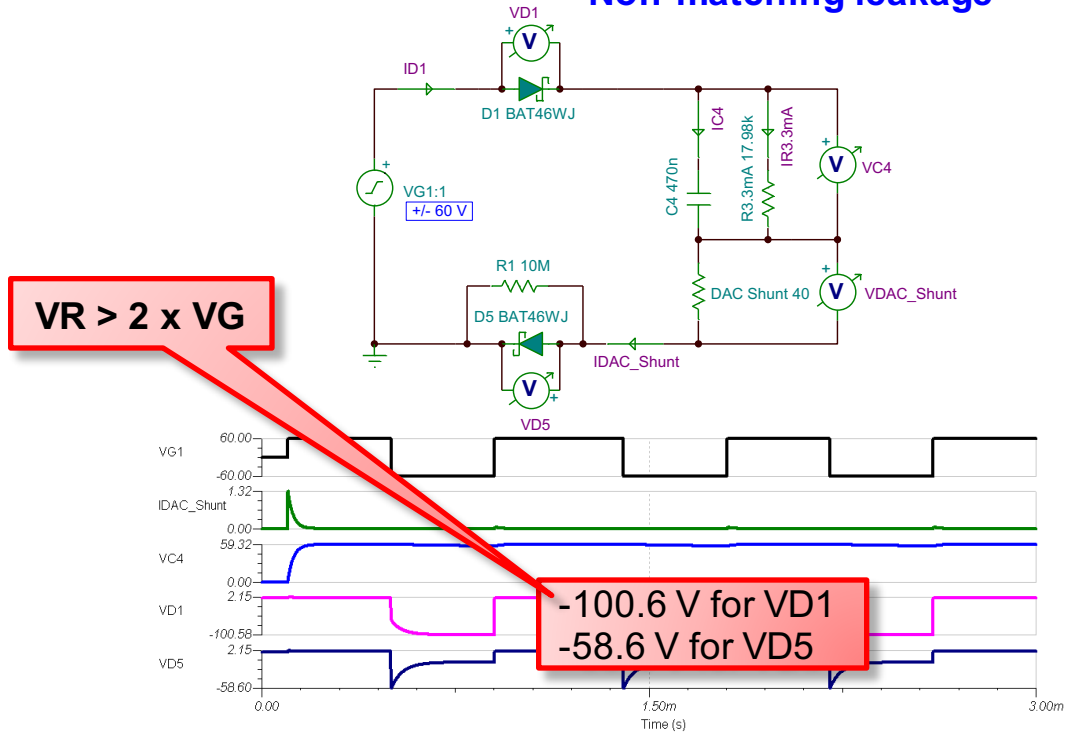
Reverse Polarity Protection – Different Approaches (II)

- Reverse leakage of diodes shows large variations, b/w typ and max values
- Min values not even given

I_R	reverse current		
Conditions			
V_R = 75 V			
V_R = 75 V; T_j = 60 °C			
Min	**Typ**	**Max**	**Unit**
-	1	4	µA
-	-	80	µA

- Increased Leakage of D5 simulated by paralleling R1

Half-Wave Rectification (Dual Diode)
Non-matching leakage

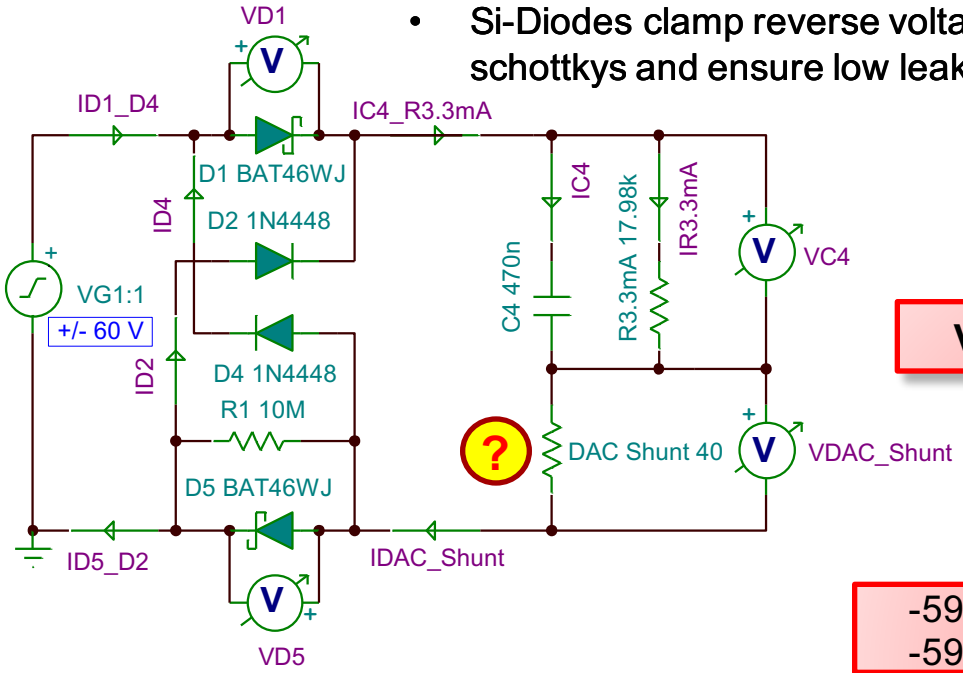


2-wire loop powered 4-20mA interface

Reverse Polarity Protection – Different Approaches (III)

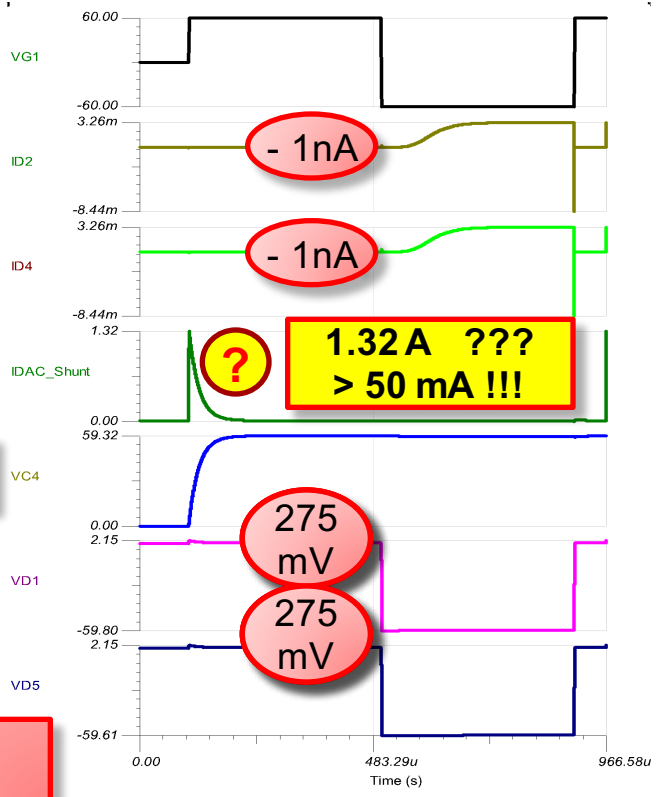
Full-Wave Rectification (Graetz Bridge)
Non-matching leakage

- Schottkys ensure low voltage losses
- Si-Diodes clamp reverse voltage of schottkys and ensure low leakage



VR > VG

-59.8 V for VD1
-59.6 V for VD5

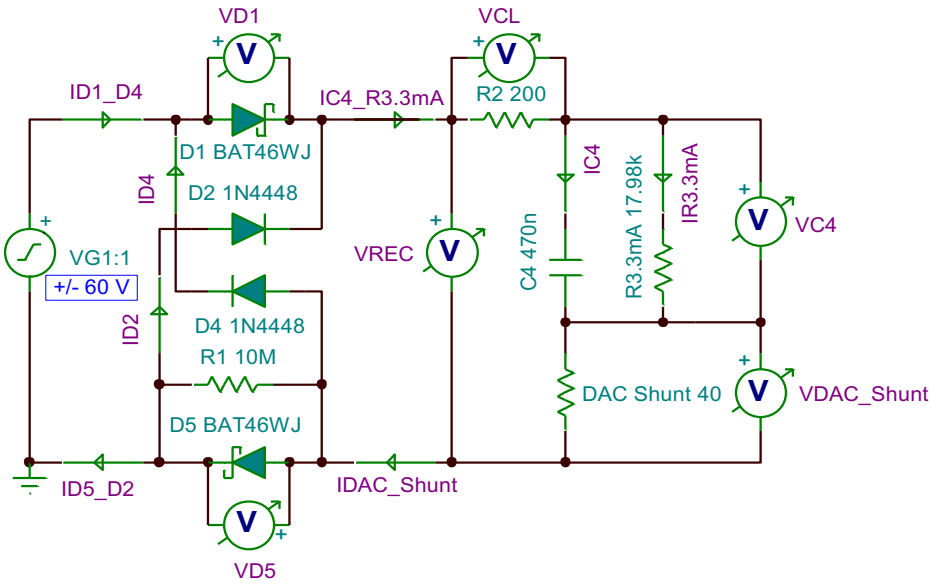


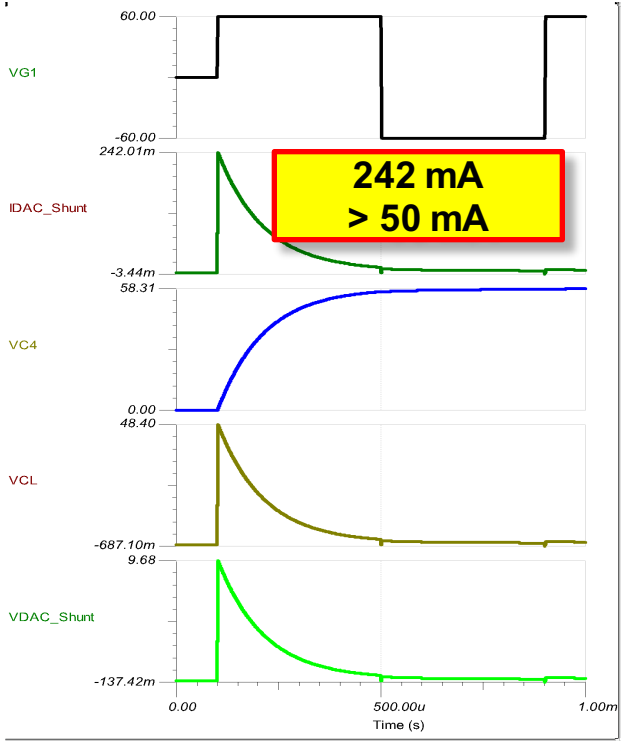
2-wire loop powered 4-20mA interface

Current Limiting – Different Approaches (I)

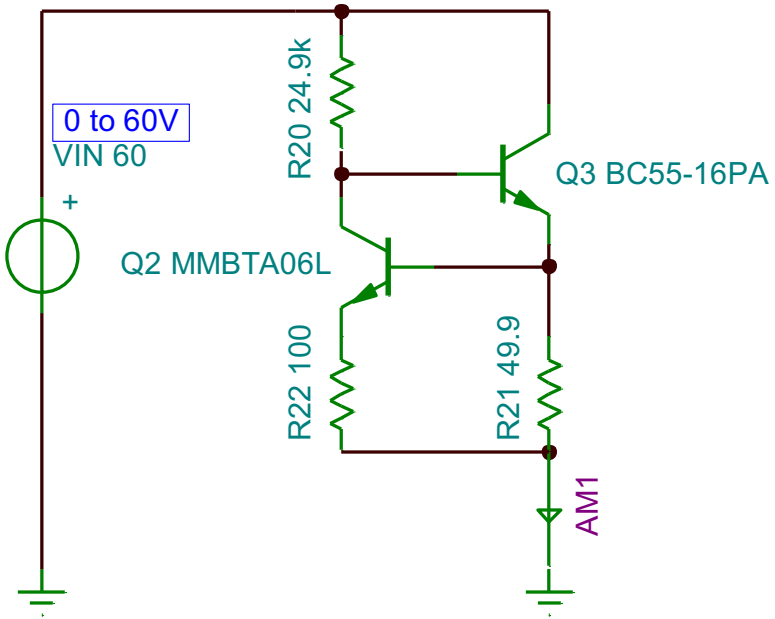
- Reduces Current Surge through the DAC's internal 40 Ω Current Shunt
  During Hot Plug and Positive Surge

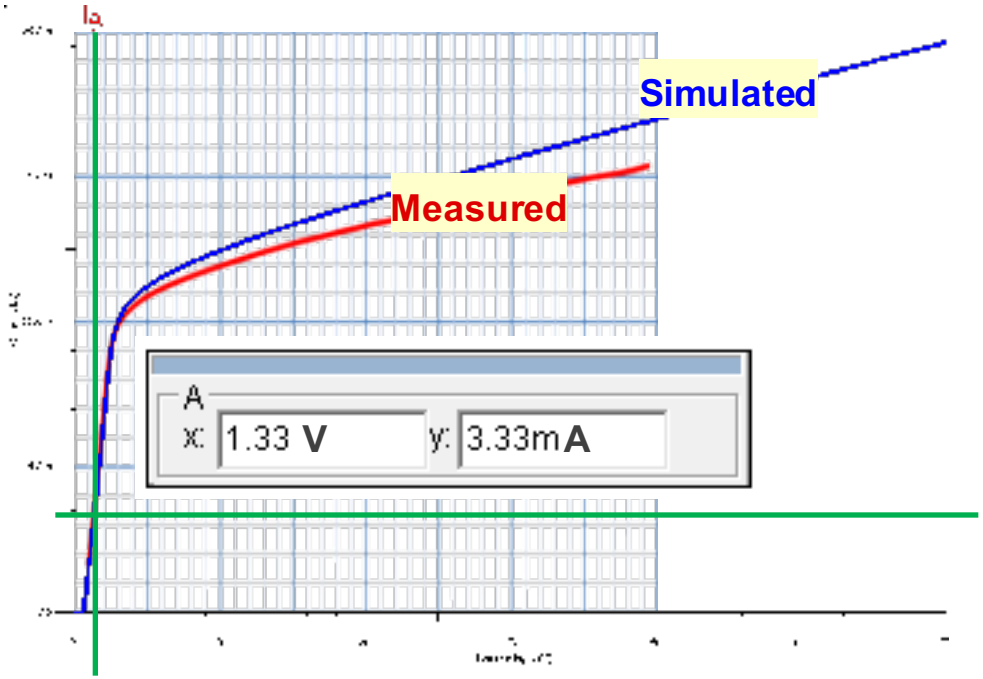
200 Ω Current Limiting Resistor





A Simple Active Current Limiter

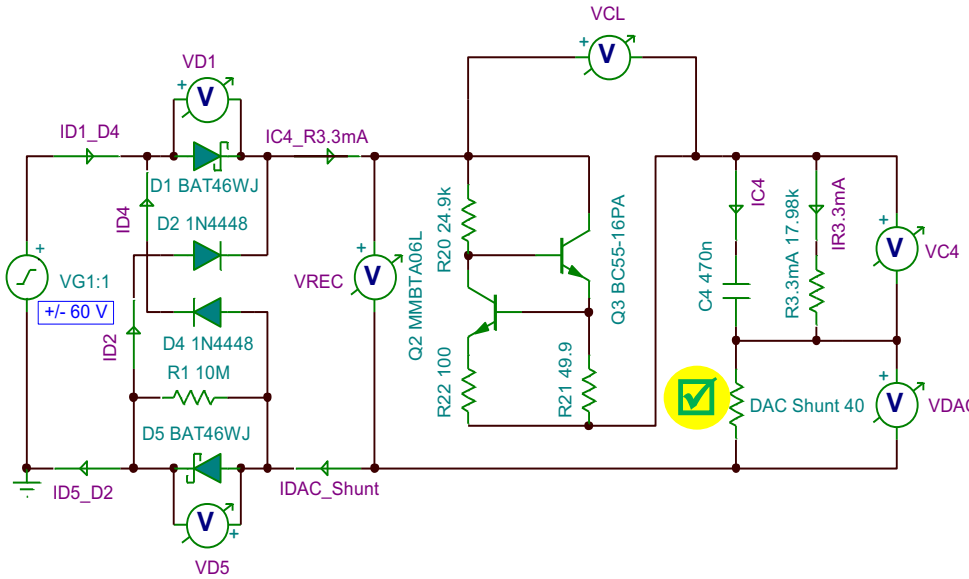


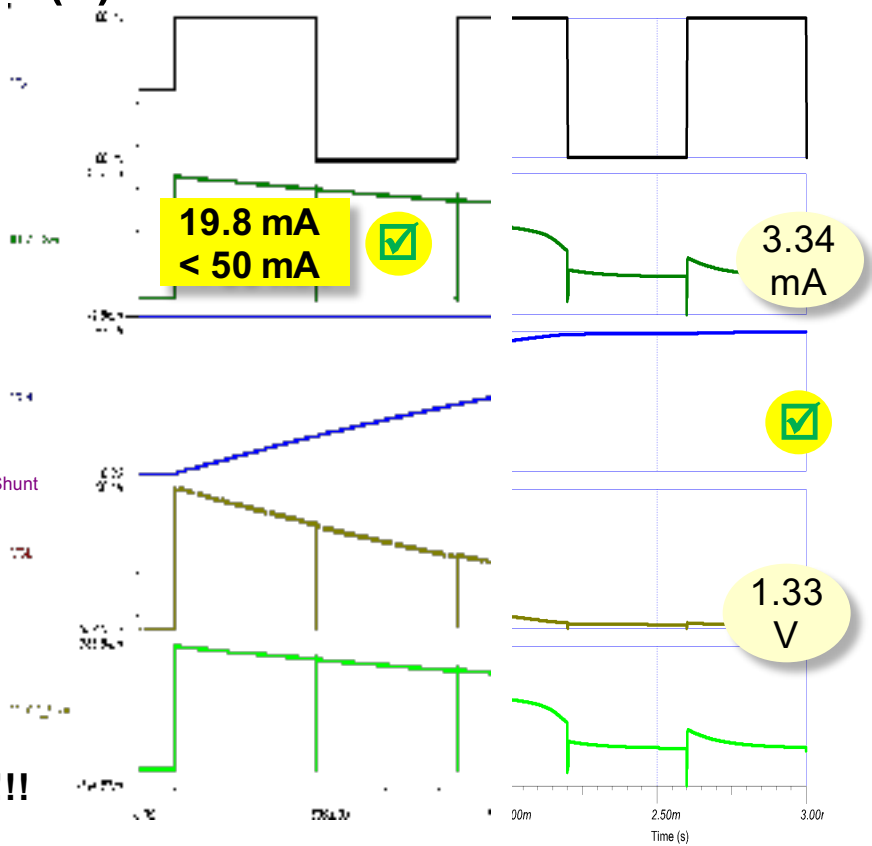


2-wire loop powered 4-20mA interface

Current Limiting – Different Approaches (II)

Active Current Limiter





- For 1.33V drop @ 3.34mA (nominal operation) a 390 Ω current limiting resistor would be needed
- **Max IDAC_Shunt: ~ 59.5 V / (390 Ω + 40 Ω) ~ 140 mA !!!**

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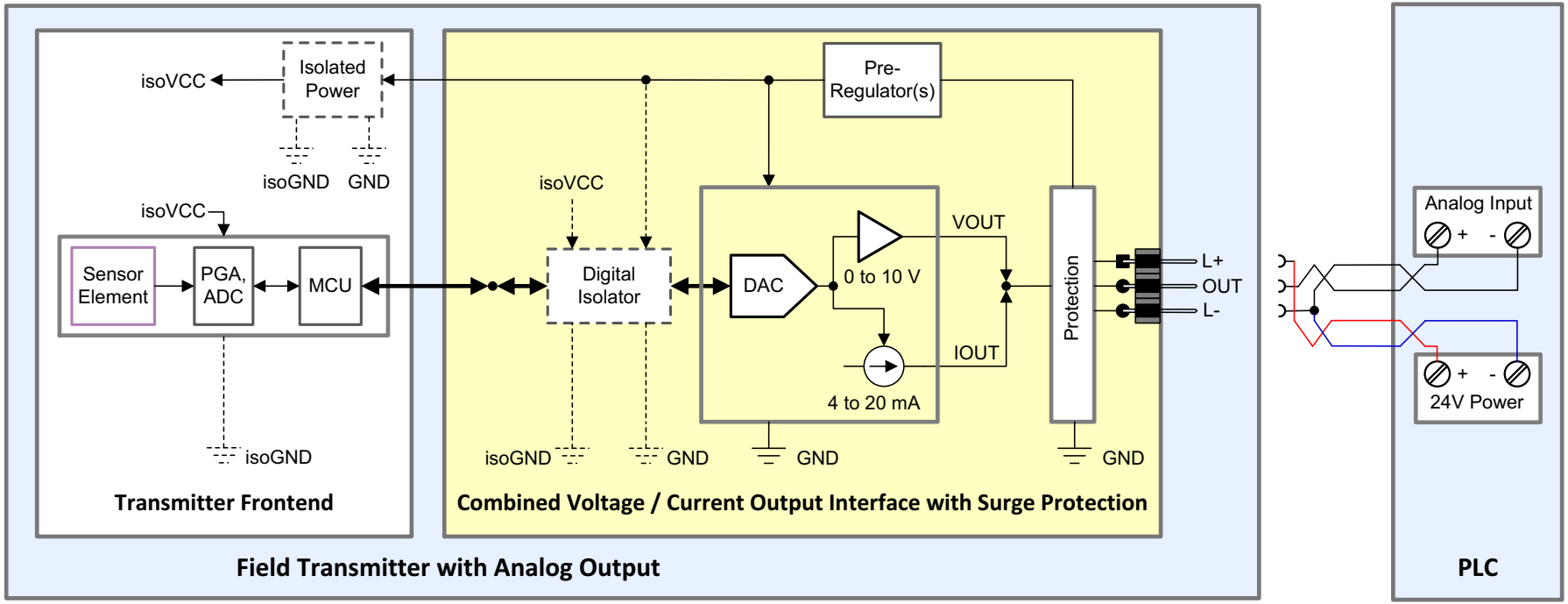
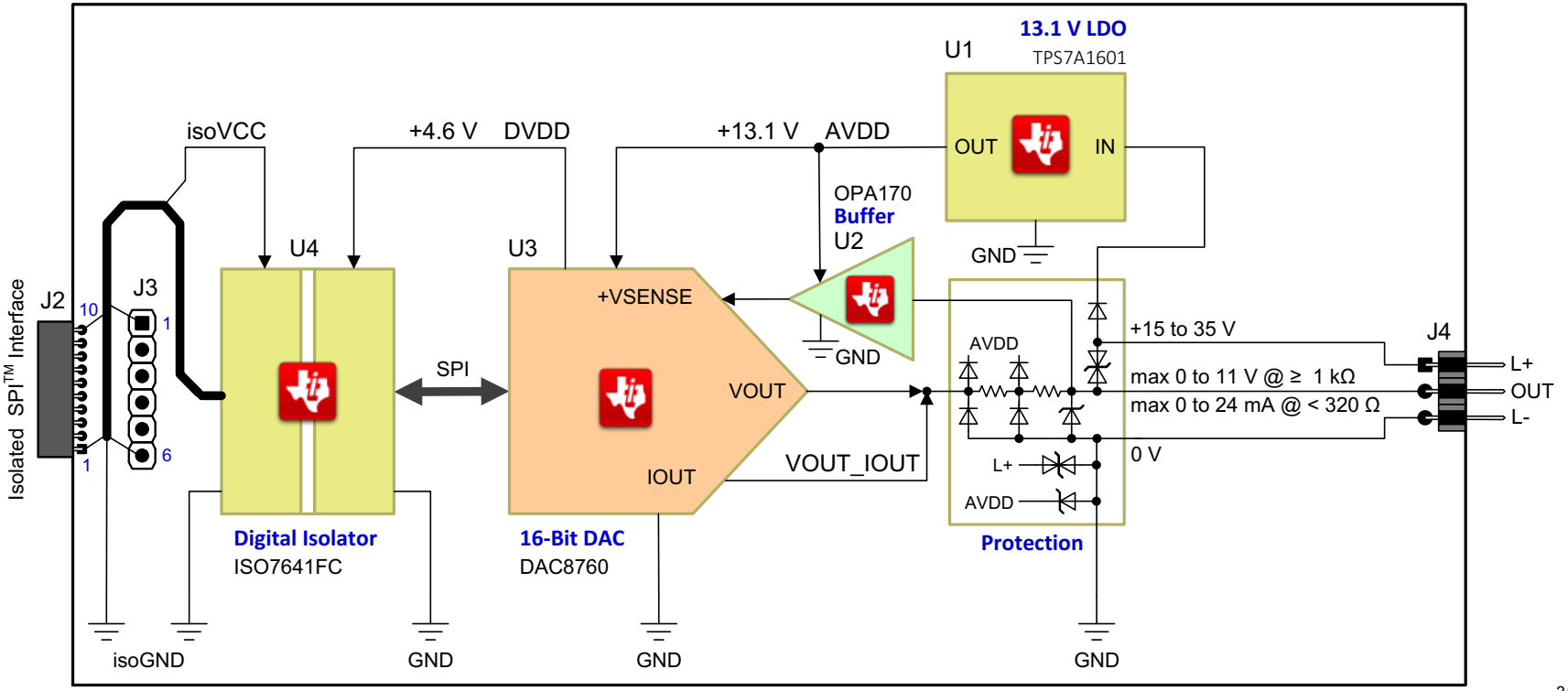
- Example implementation 2: Combined Voltage / Current output
  - Surge Protection
    - TVS Diodes
    - Current Steering Diodes + Current Limiting Resistors
  - Reverse Polarity Protection
  - Clamping of internal voltage rails

  Example: TIDA-00559

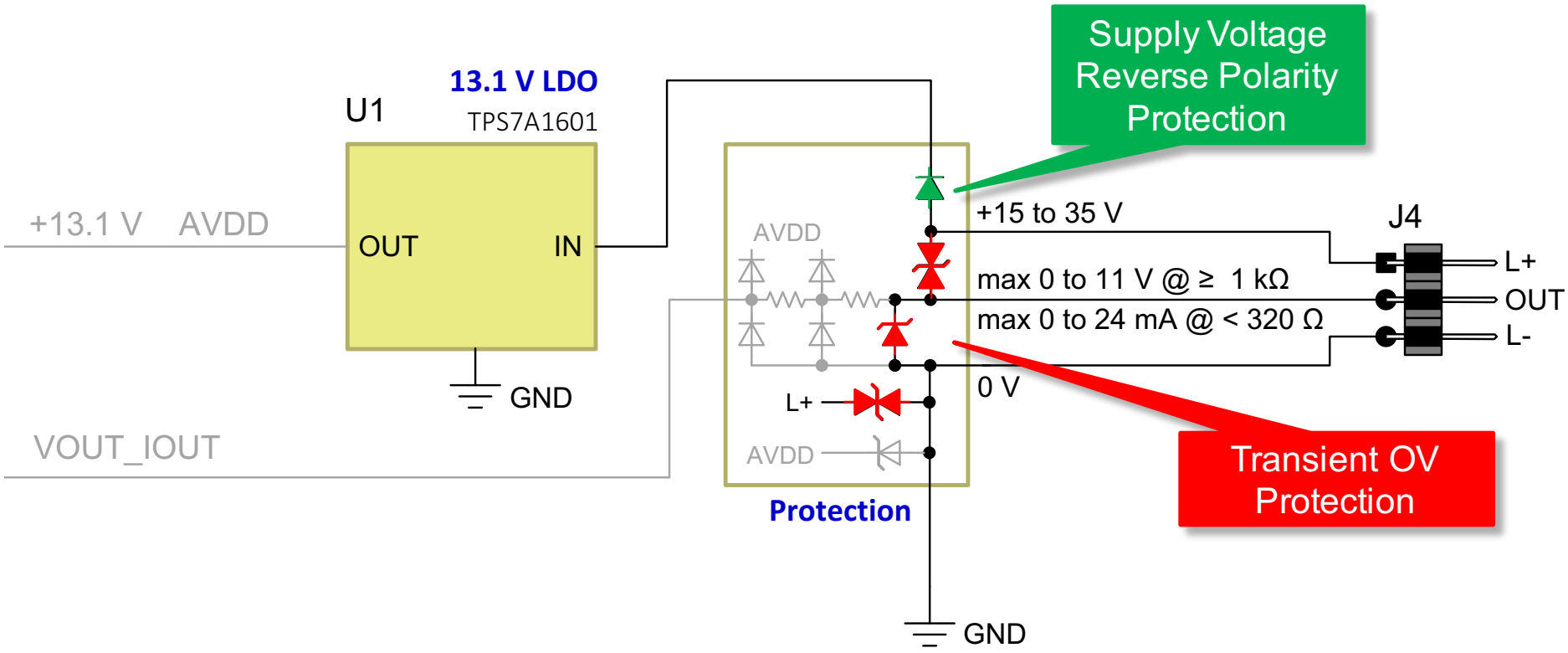
TIDA-00559: Combined Voltage / Current Interface Systems View



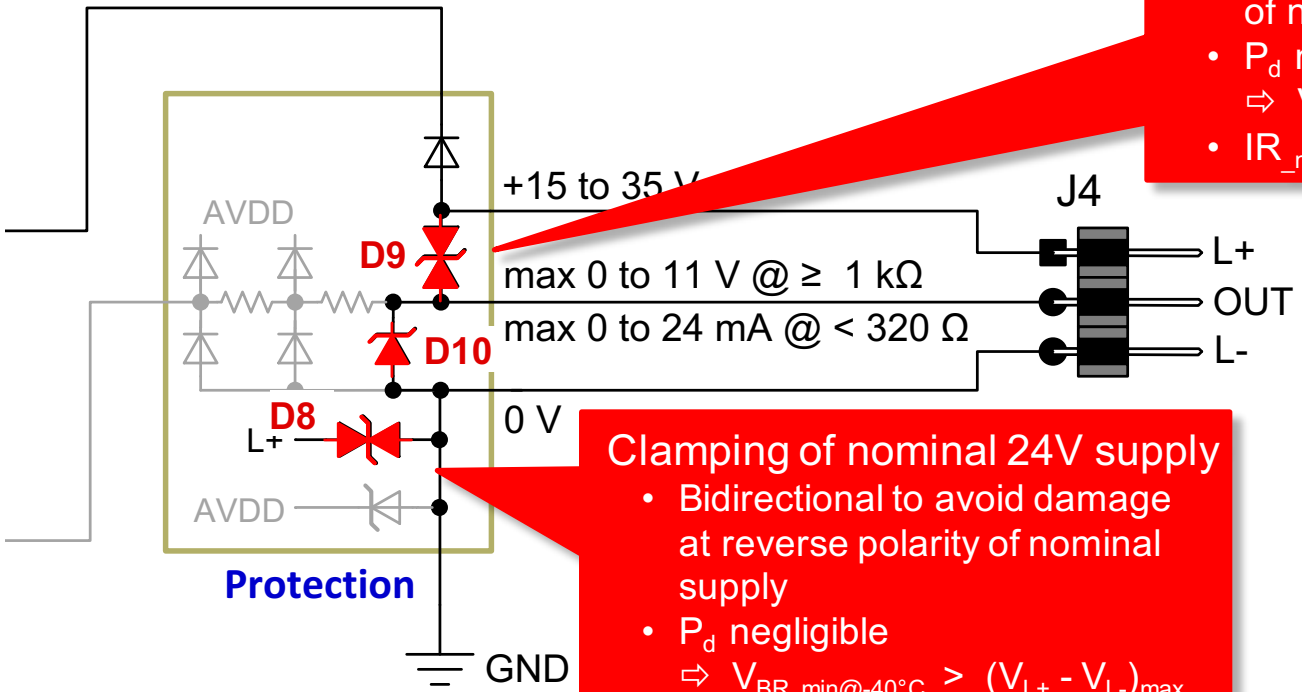
TIDA-00559: Combined Voltage / Current Output Detailed Block Diagram



Combined Voltage / Current Output Basic Protection on Interface Connector



Basic Protection on Interface Connector
Transient OV Protection - Details



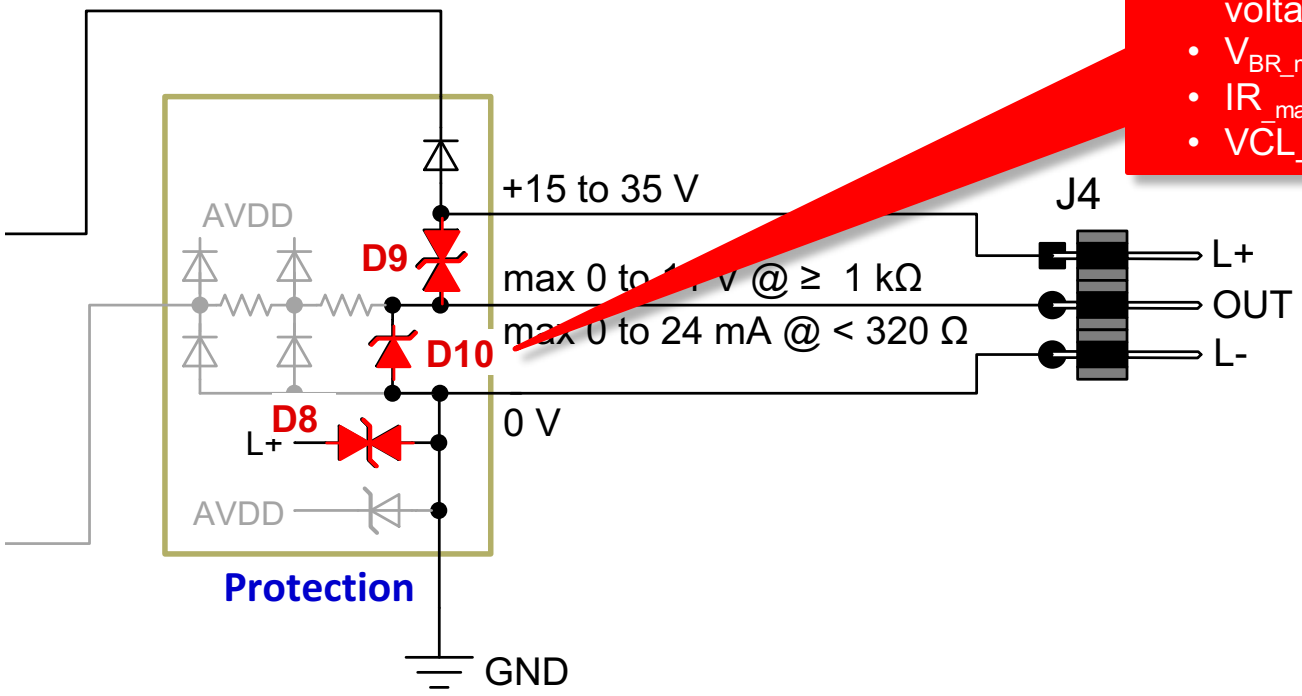
Voltage Clamping b/w L+ and OUT

- Bidirectional to avoid damage of D9 and D10 at reverse polarity of nominal supply
- P_d negligible
  ⇨ $V_{BR\_min@-40°C}$ > 35 V
- $IR_{\_max@+85°C,\ 35V}$ < 1 µA

Clamping of nominal 24V supply

- Bidirectional to avoid damage at reverse polarity of nominal supply
- P_d negligible
  ⇨ $V_{BR\_min@-40°C} > (V_{L+} - V_{L-})_{max}$
- $V_{CL\_max@+100°C} < VIN_{max\_U1}$

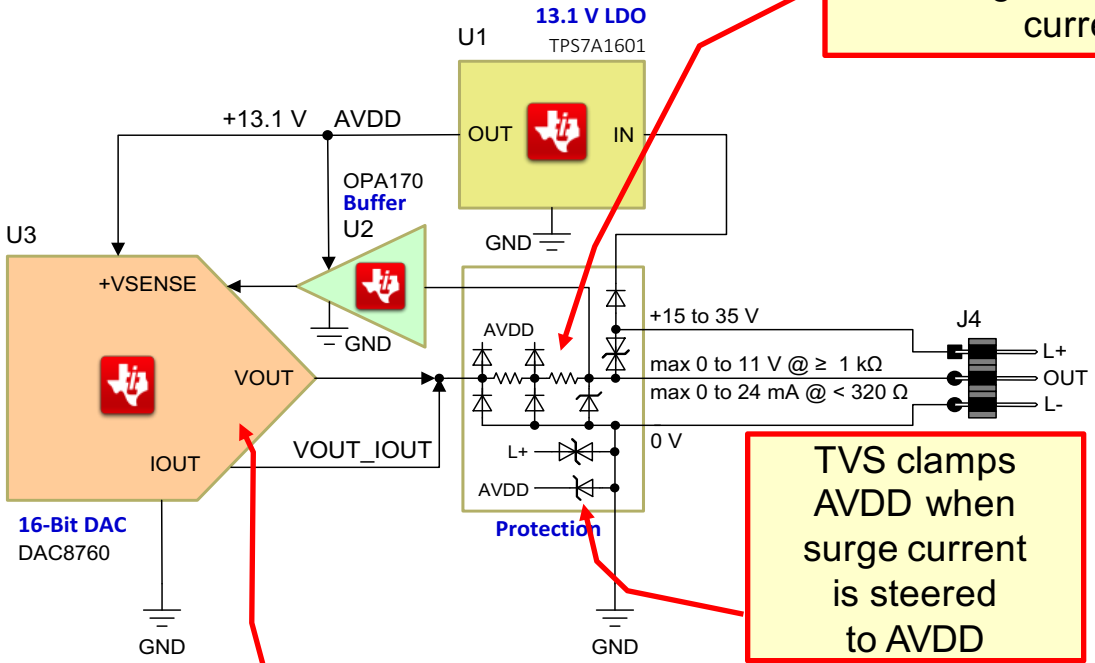
Basic Protection on Interface Connector
Transient OV Protection - Details



Voltage Clamping b/w OUT and L-

- Unidirectional fits best the unipolar voltage range on OUT
- $V_{BR\_min@-40°C}$ > AVDD
- $IR_{\_max@+85°C,\ 7.7V}$ < 1 µA
- VCL_max@+125°C < AVDD

Protection of output pins of the 16-Bit DAC

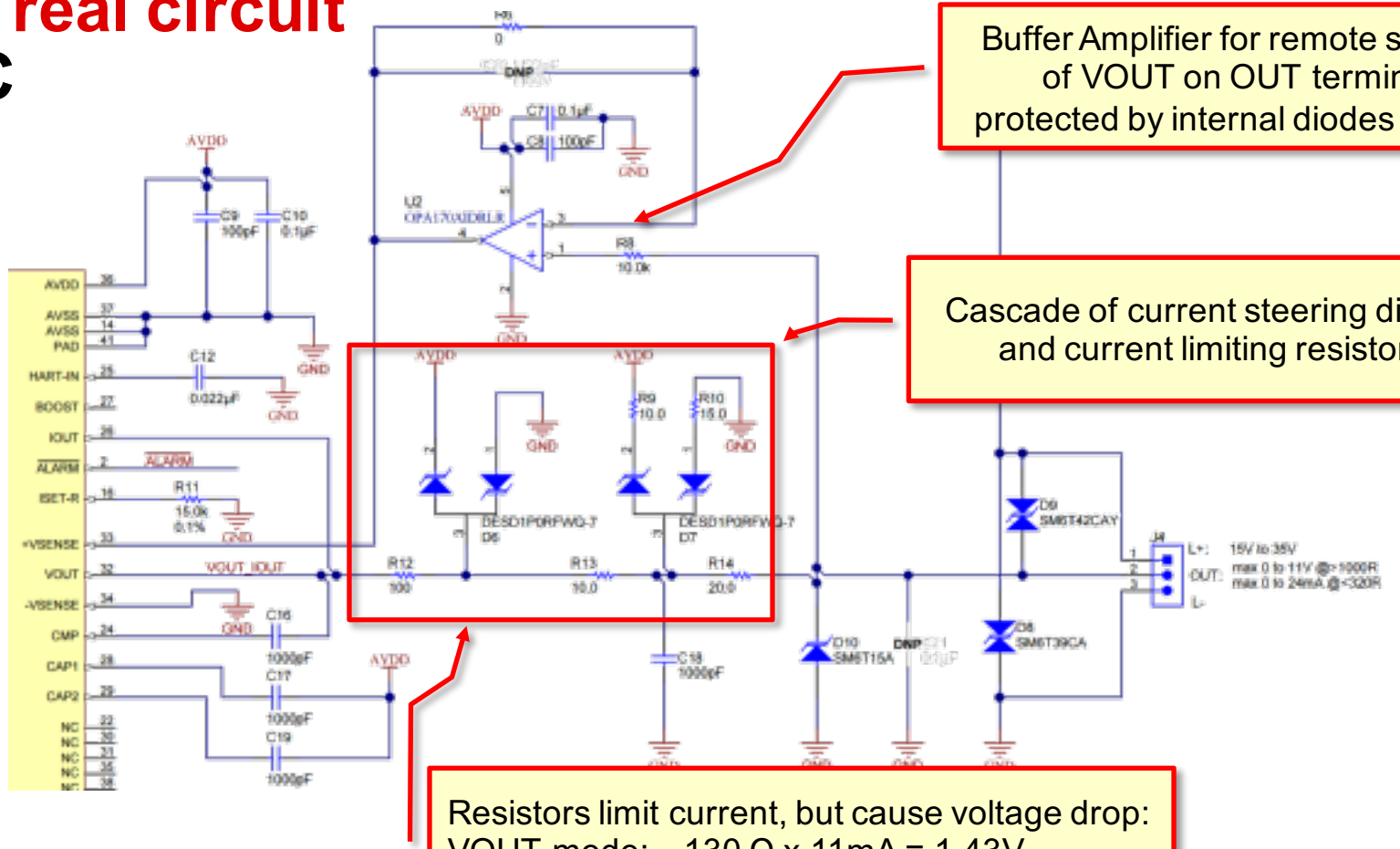


Steering diodes steer current to AVDD or GND, current is limited by resistors

TVS clamps AVDD when surge current is steered to AVDD

Voltages on IOUT & VOUT must not exceed AVDD nor go below GND or current needs to be limited

The real circuit
DAC



Effects of current limiting resistors:
How to deal with the voltage drops ?

- **VOUT mode:**
  - Buffer Amplifier for remote sensing compensates for voltage drops
  - Need for increased footroom when sinking current into VOUT
    - Can be addressed by bipolar supply of DAC
- **IOUT mode:**
  - Worst case drop of 3.12V reduces significantly the maximum achievable output voltage and therefore the maximum usable load resistance in the loop:
    - AVDDtyp: 13.12 V

AVDD_min:	12.84 V
- VCOMPLIANCE_max	2.00 V
- VDROP on c/l resistors	3.12 V
VOUT_max on J4	7.72 V

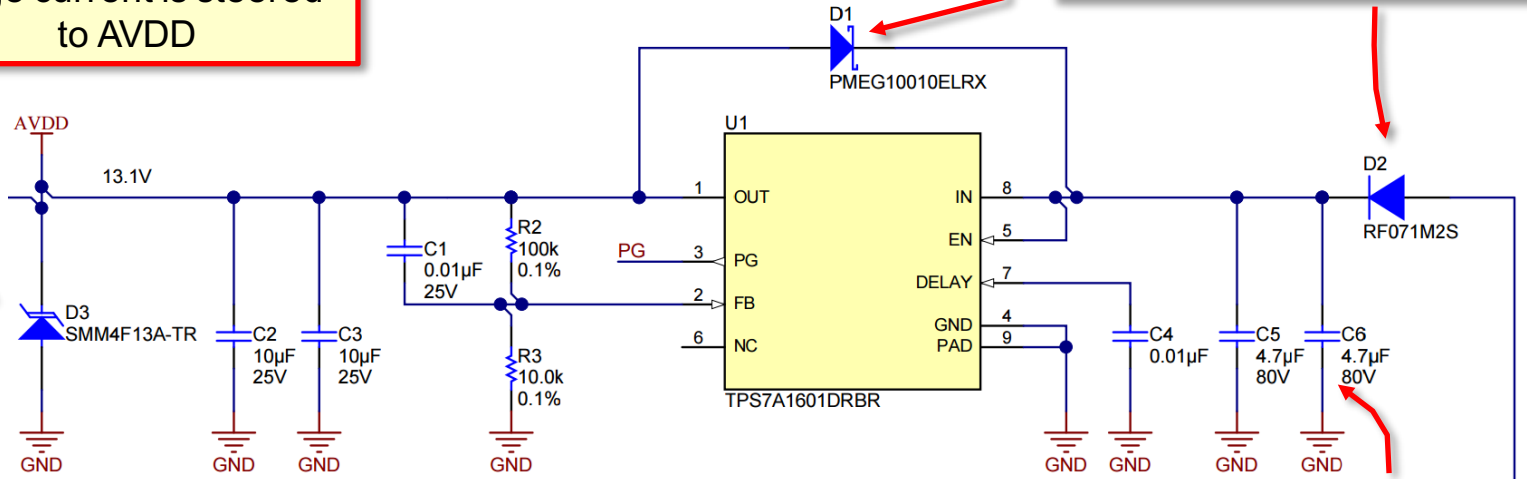
    - RLOAD_max = VOUT_max on J4 / IOUT_max = 7.72V / 24 mA = 321.7 Ω

The real circuit
LDO

Protects LDO's internal FET when not powered, but surge is applied b/w OUT and L- of J4

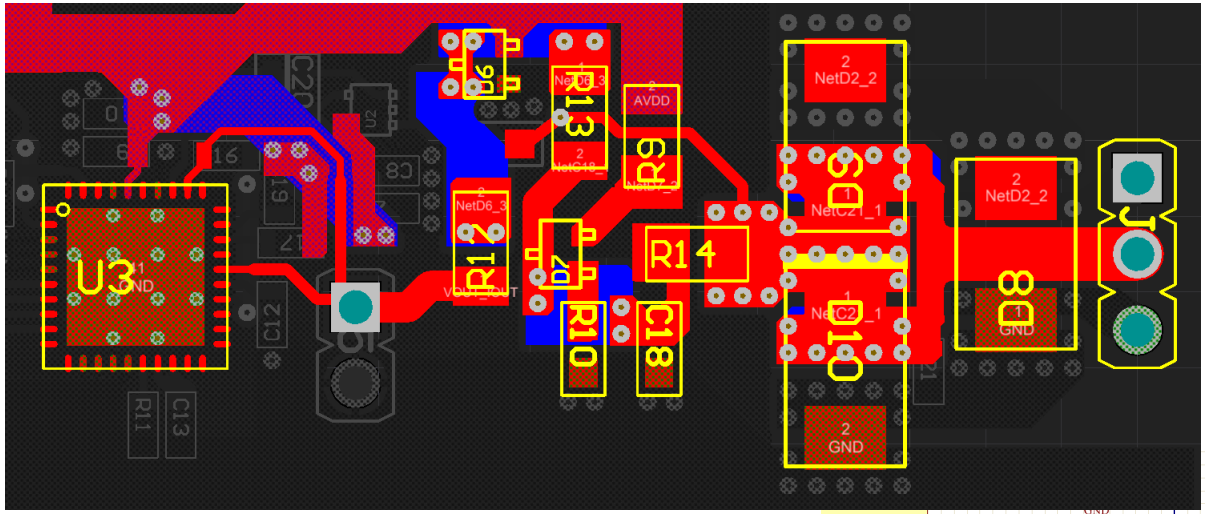
TVS clamps AVDD when surge current is steered to AVDD

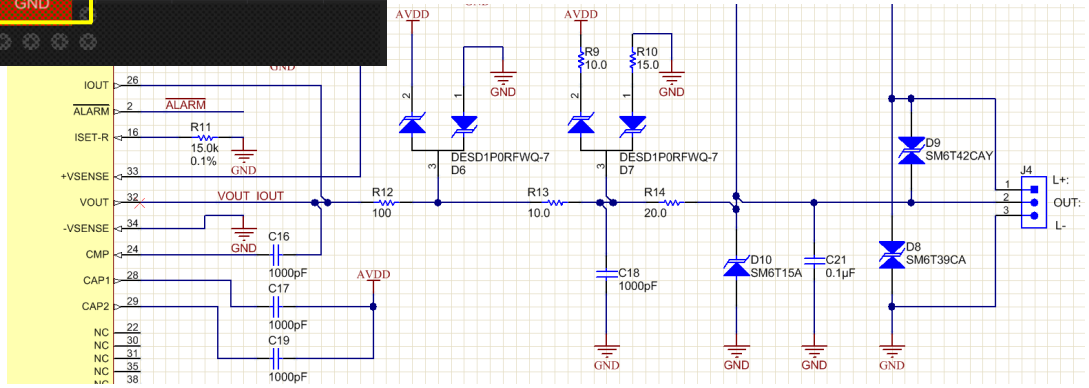
Reverse Input protection for LDO



LDO Input Bypass Caps,
Stored energy avoids
System Reset during negative surge

Layout Example TIDA-00559





Conclusion

- Introduction to IEC61000-4 EMC Immunity Test Suite
  - Surge Immunity test is the most severe.
  - TVS diode as countermeasure
- Surge Protection with TVS Diode and implications for the system
  - Understanding of TVS parameters and characteristic
  - Selection process of TVS
- Example Implementations:
  - Loop-powered 4-20mA Transmitter
  - Combined Voltage / Current output
  - Practical protection circuits and their side effects

Thank You!

Questions?