汽车DCDC芯片EMC设计要点与PCB layout优化

07/03/2019

rev 20180504

目录

- 1.汽车DCDC芯片EMC的主要内容和趋势
- 2.汽车DCDC芯片EMC特性
- 3.汽车DCDC芯片EMC的设计要点
- 4.汽车DCDC芯片EMC抑制措施
- 5:BUCK 电源的PCB优化设计范例

汽车新趋势对电源提出了新的要求

更多的电源需求，更大的功耗，更小的体积对汽车DCDC电源的EMC设计带来更加严峻的挑战

我们可以看到汽车发展的趋势，
电气化进程进一步加剧，新能源车快速增长，车载互联开始增多，
自动驾驶的部件开始慢慢安装起来，
这里面就有更多的ECU，更多的通讯部件，更大的功耗，传统的LDO已经不能满足功耗和效率的要求，
我们看到了更多的DCDC需求，对部件中的DCDC EMC设计带来更多严峻的考验。

汽车电子设备的EMC测试内容

零部件测试类别			测试项目	ISO	CISPR	GB	频率
EMC	EMI	CE	电源线时域传导发射	7637-2		GB/T21437	
			电源线频域传导发射		CISPR25	18655	150K~108M
			信号线频域传导发射		CISPR25	18655	
		RE	辐射发射-天线接收法		CISPR25	18655	150K~1G
			辐射发射-TEM小室法		CISPR25	18655	
	EMS	CS	电源线脉冲抗扰度	7637-2		GB/T21437	
			信号线脉冲抗扰度	7637-3		GB/T21437	
			RF能量直接注入	11452-7			250K~400M
			大电流注入（BCI）	11452-4		17619	1M~400M
			电源线音频耦合抗扰度				
		RS	辐射抗扰度-天线照射法	11452-2		17619	80M~18G
			辐射抗扰度-TEM小室法	11452-3		17619	10Khz~200M
			辐射抗扰度-带状线法	11452-5		17619	10K~400M
			辐射抗扰度-磁场环照射法	11452-8			15K~30K
		ESD	静电放电实验	10605		19951	

目录

- 1.汽车DCDC芯片EMC的主要内容和趋势
- 2.汽车DCDC芯片EMC特性
- 3.汽车DCDC芯片EMC的设计要点
- 4.汽车DCDC芯片EMC抑制措施
- 5:BUCK 电源的PCB优化设计范例

EMC三要素

干扰源　　耦合路径　　敏感设备

在EMI测试中，待测零部件是干扰源，LISN和天线是敏感设备，通过LISN和天线接收信号来分析零部件的电磁干扰的水平
在EMS测试中， 通过各种天线对零部件发射电磁信号，以及在零部件输入端注入脉冲和噪声，来评估零部件的抗扰能力

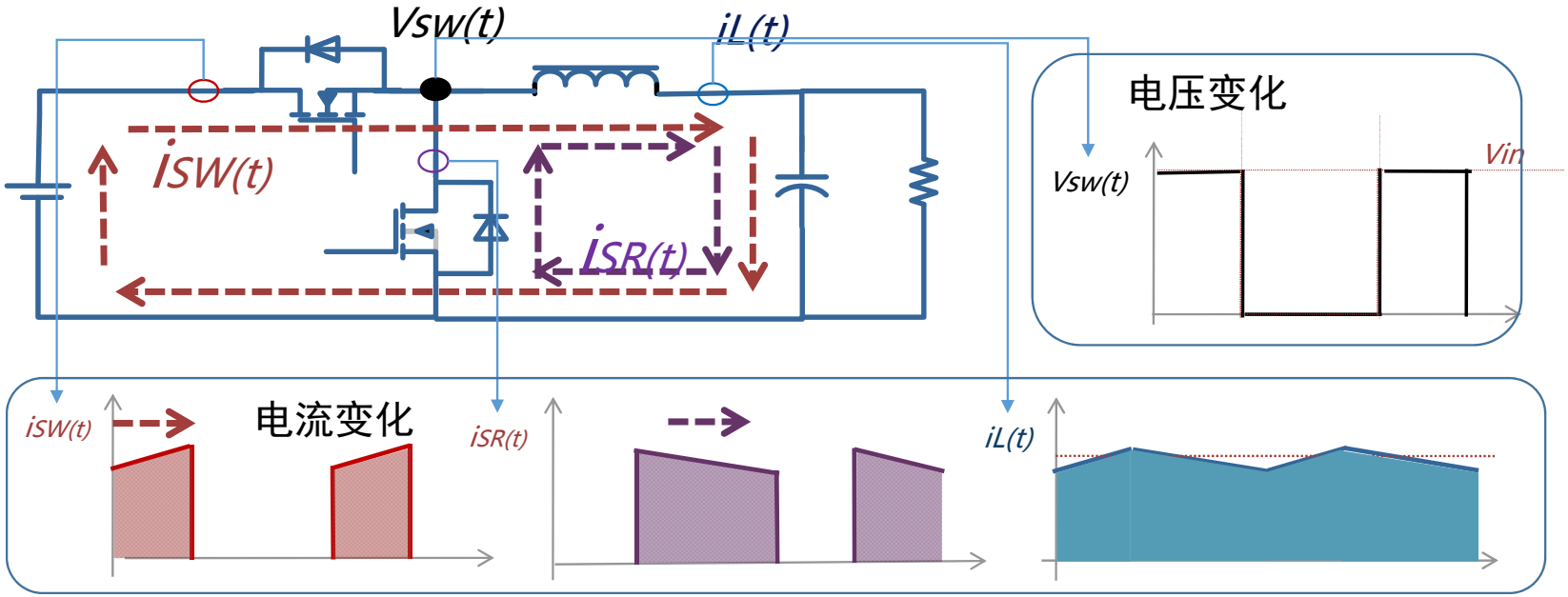
因为DCDC芯片是最常见的干扰源，而通常又不易受干扰（偶尔也会受到干扰，FB电阻值过大被干扰到）。
DCDC芯片的EMC问题主要就是EMI问题

这三个要素， 假如任何一个不存在，就不会有EMC问题。

DCDC芯片的噪声特性

开关电源中噪音的根源： 快速的turn on和turn off而产生的电压和电流方波，以及二极管反向恢复特性， 所产生的di/dt和dv/dt 的方波， 其高速的di/dt和dv/dt， 而产生EMI的源头。

BUCK电路的常见开关波形：



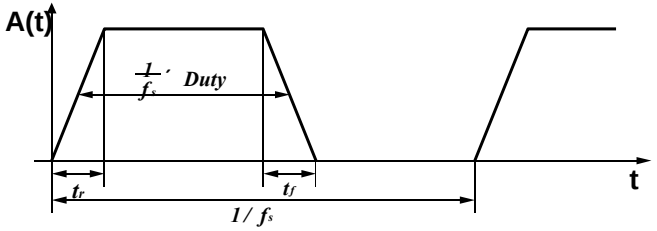
以BUCK为例，DCDC芯片开关过程中产生电压和电流的变化，包含了较快的di/dt和dv/dt噪声分量.
我们将上图中的方波进行傅里叶分析，得到下一页：

当然对于其他结构电源，比如反激， PFC，BOOST， BUCK/BOOST等电路，当了解工作原理后， 先寻找到di/dt和dv/dt

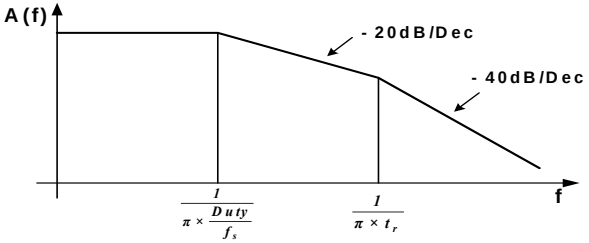
DCDC芯片噪声的频率特性

噪声的傅里叶分析

时域

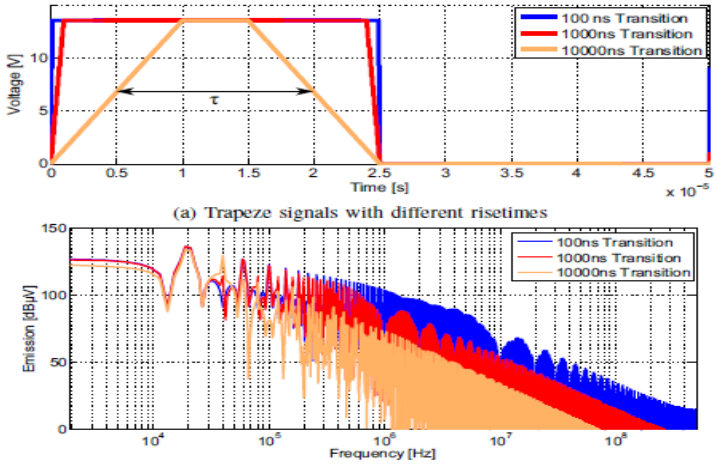


频域



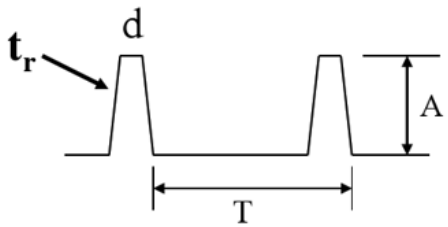
以BUCK为例，DCDC芯片开关噪声不仅包含开关次和倍频频率段的噪声，还根据开关速度不同会产生更高频的噪声

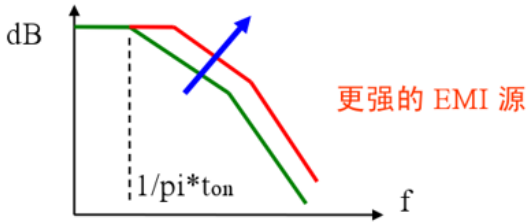
噪声源和开关速度斜率



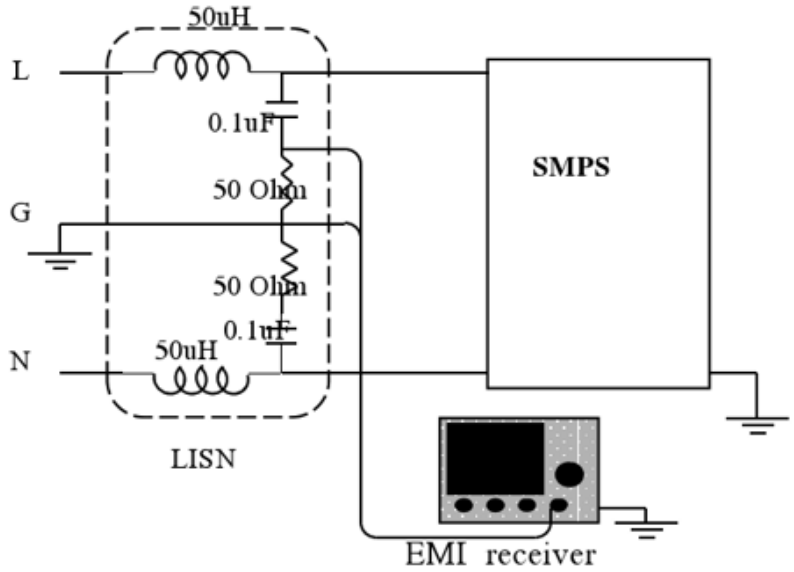
上图中个三个波形的，基频幅度基本一致，但是随着dv/dt或者di/dt的斜率的不同，高频的db数值会有较大影响。(减小斜率改善）

*更高的工作频率、更高的dv/dt、di/dt，**更强高频频谱！***

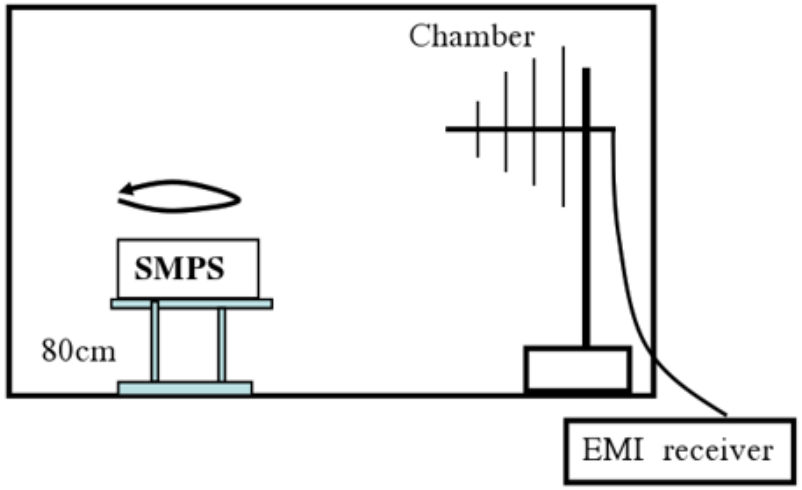




DCDC芯片噪声的传导和辐射耦合路径



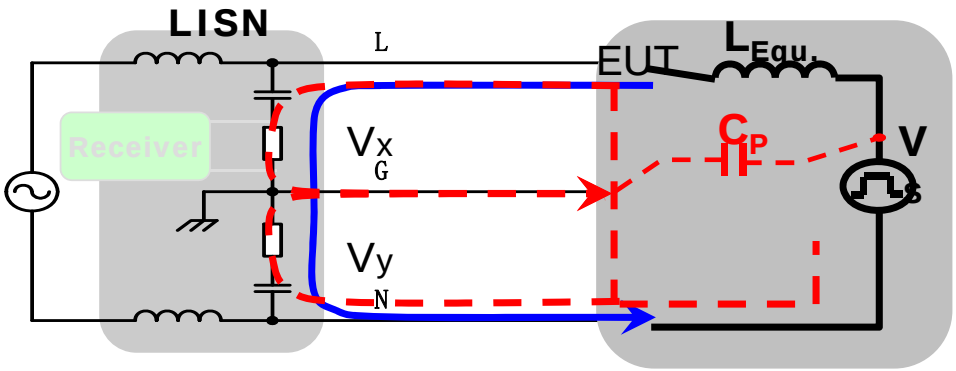
传导测试测试



辐射发射测试

DCDC芯片噪声的传导耦合路径

传导噪声的分类和耦合路径



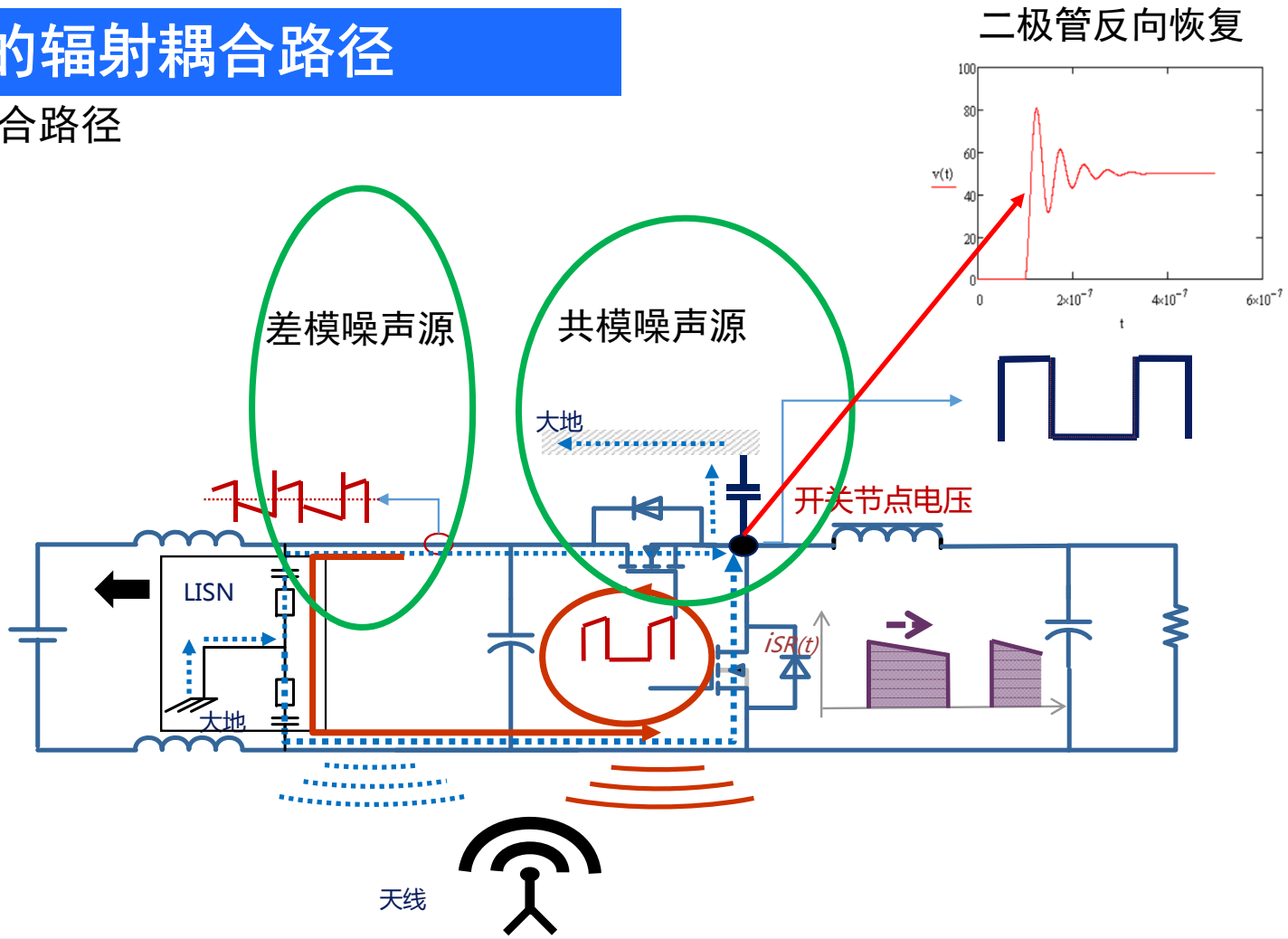
- 差模噪声 $V_{DM}=(V_x-V_y)/2.$
- 共模噪声 $V_{CM}=(V_x+V_y)/2$

简单的说，差模噪声是LN线之间的电位差，共模噪声是待测零部件的LN线和参考地之间的电位差

我们将上图进行细化， 得到：

DCDC芯片噪声的辐射耦合路径

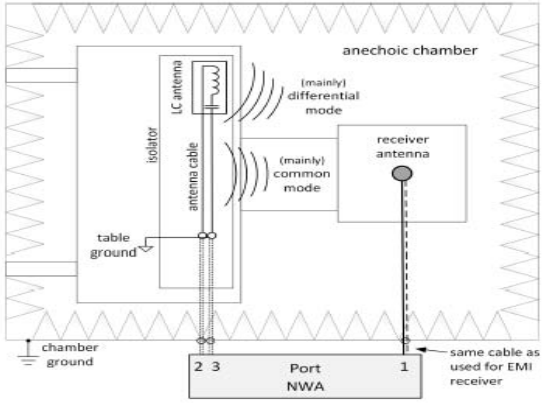
DCDC芯片的噪声和耦合路径

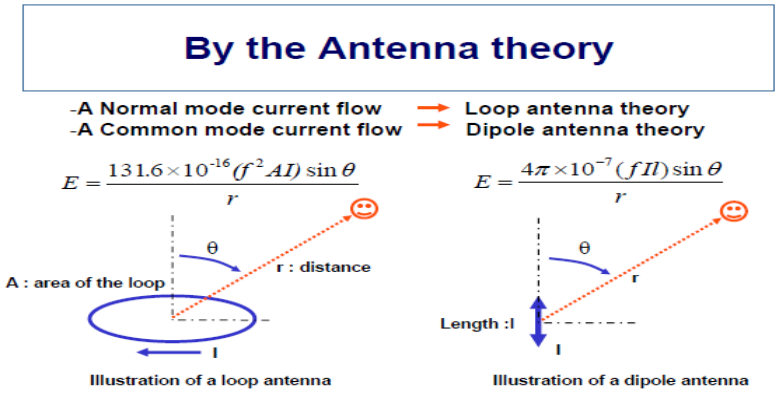


DCDC电源EMI的主要来源于电流和电压跳变，通过共模和差模的形式耦合到接收器上（LISN和天线）

DCDC芯片噪声的辐射耦合路径

辐射噪声的分类和耦合路径





辐射噪声也可分为差模和共模辐射噪声，可通过小环天线和偶极子天线原理来估算

目录

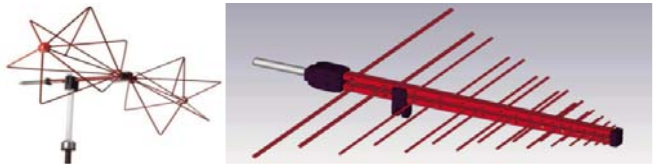
- 1.汽车DCDC芯片EMC的主要内容和趋势
- 2.汽车DCDC芯片EMC特性
- 3.汽车DCDC芯片EMC的设计要点
- 4.汽车DCDC芯片EMC抑制措施
- 5:BUCK 电源的PCB优化设计范例

EMC设计三要素

干扰源

耦合路径

敏感设备



抑制干扰源

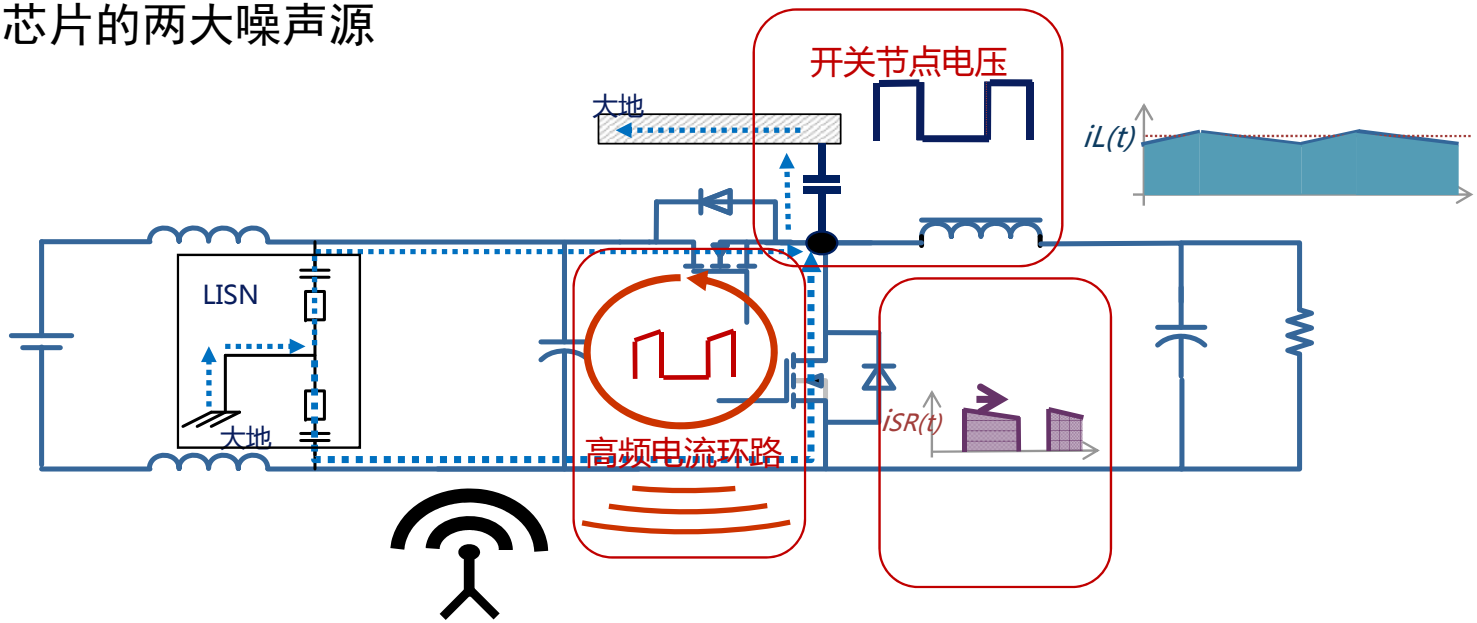
切断耦合路径

保护敏感设备

EMI设计的三大基本原则，也是最重要的原则。

DCDC芯片的噪声源

DCDC芯片的两大噪声源

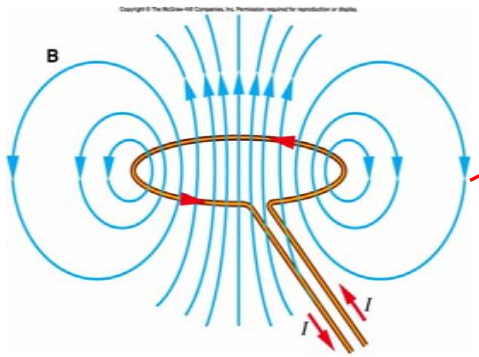


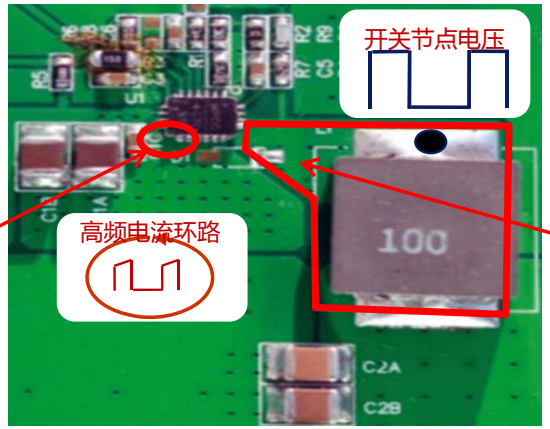
DCDC芯片的主要噪声源是高频电流环路(Hot loop)和高频开关节点(SW note)，包含了比较宽频段的谐波分量

DCDC芯片的高频电流环路

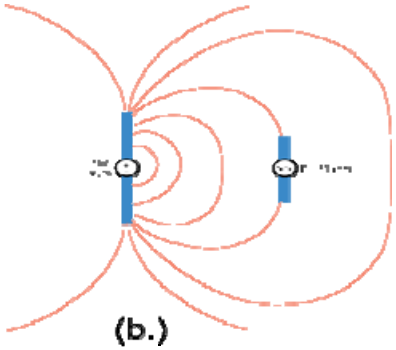
DCDC芯片的两大噪声源

di/dt环路会产生磁场





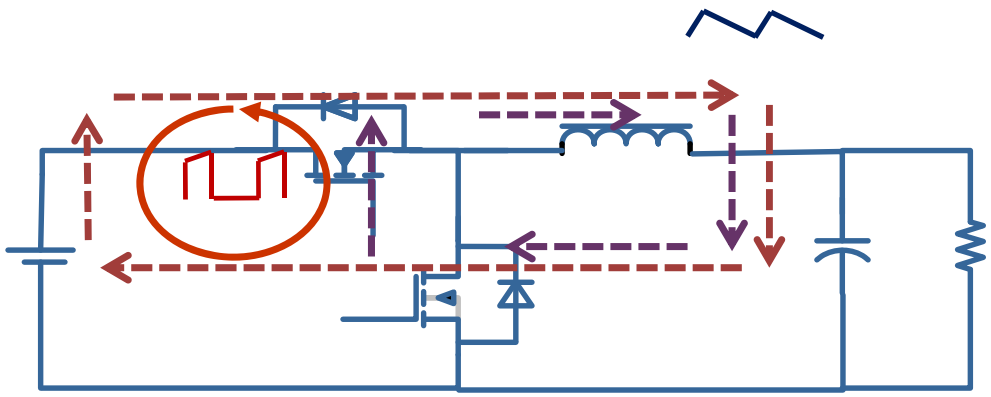
dv/dt节点会产生电场

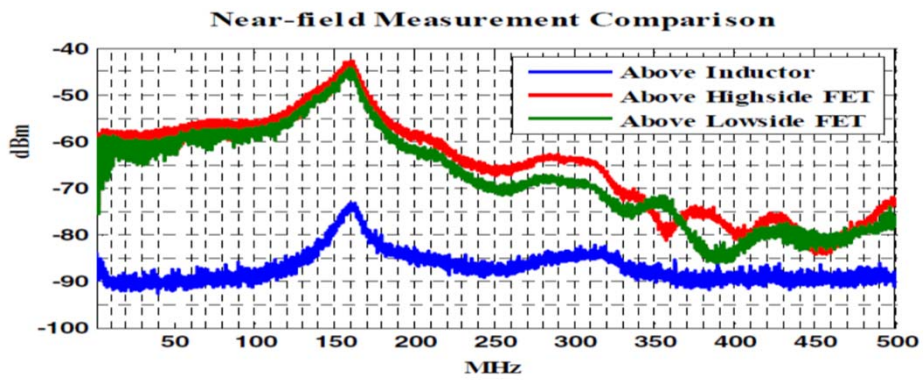


高频电流环路(Hot loop)和高频开关节点(SW note)分别产生交变的磁场和电场

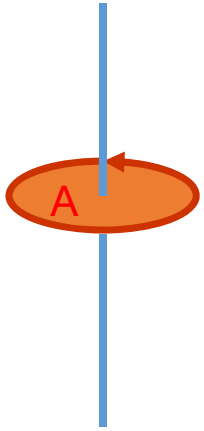
高频电流环路和磁场

高频电流环路的近场磁场强度要高于电感附近





© Keong W. Kam, David Pommerenke Cheung-Wei Lam, Robert Steinfeld
EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis



高频电流环路可以看成是磁偶极子，磁矩 $\mu = I * A$

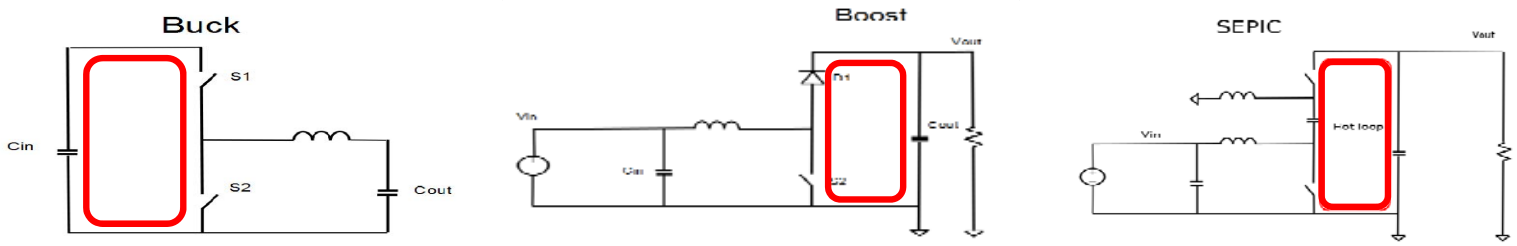
磁场强度随着电流和环路面积而增大。

高频电流环路形成的磁场大小取决于环路面积和电流大小

正确的找出高频电流环路

各种拓扑的高频电流环路

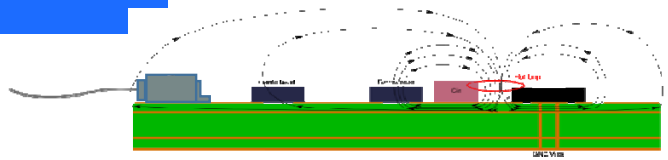
存在于开关回路和滤波电容之间，需要重点关注。
而电感电流是连续的三角波波形，相对而言不是关注的重点



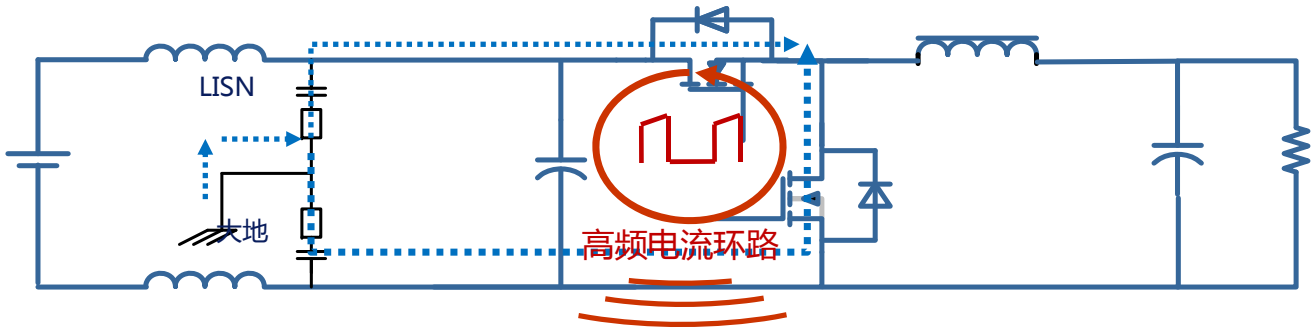
©Christian Kueck &Jens Hedrich

高频电流环路主要存在于电流切换的支路，开关管和连接在开关端两端的电容组成了高频电流回路。

高频电流环路的辐射能量



环路天线原理



$$E = \frac{263\ e^{-16} \times f^{2} \cdot I \cdot A}{r}$$

E: electro magnetic field energy
A: loop area of the high di/dt current path

高频电流环路的辐射能量取决于环路面积和电流大小

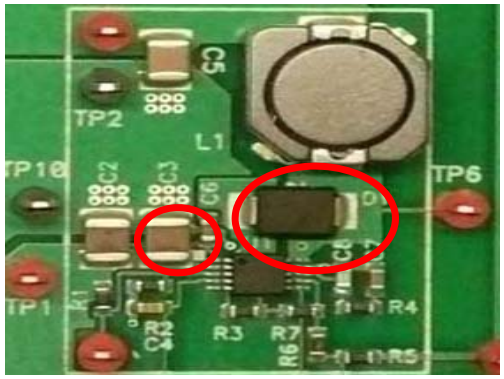
目录

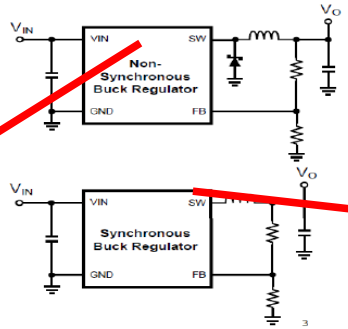
- 1.汽车DCDC芯片EMC的主要内容和趋势
- 2.汽车DCDC芯片EMC特性
- 3.汽车DCDC芯片EMC的设计要点
- 4.汽车DCDC芯片EMC抑制措施
- 5:BUCK 电源的PCB优化设计范例

高频电流环路噪声源的抑制

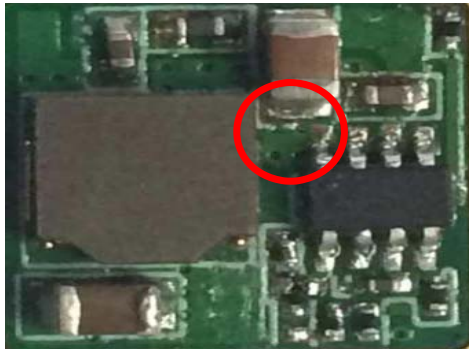
1. 同步方案减少高频电流回路面积

非同步buck方案





同步buck方案，
少了肖特基二极管，
同时减小了环路面积。

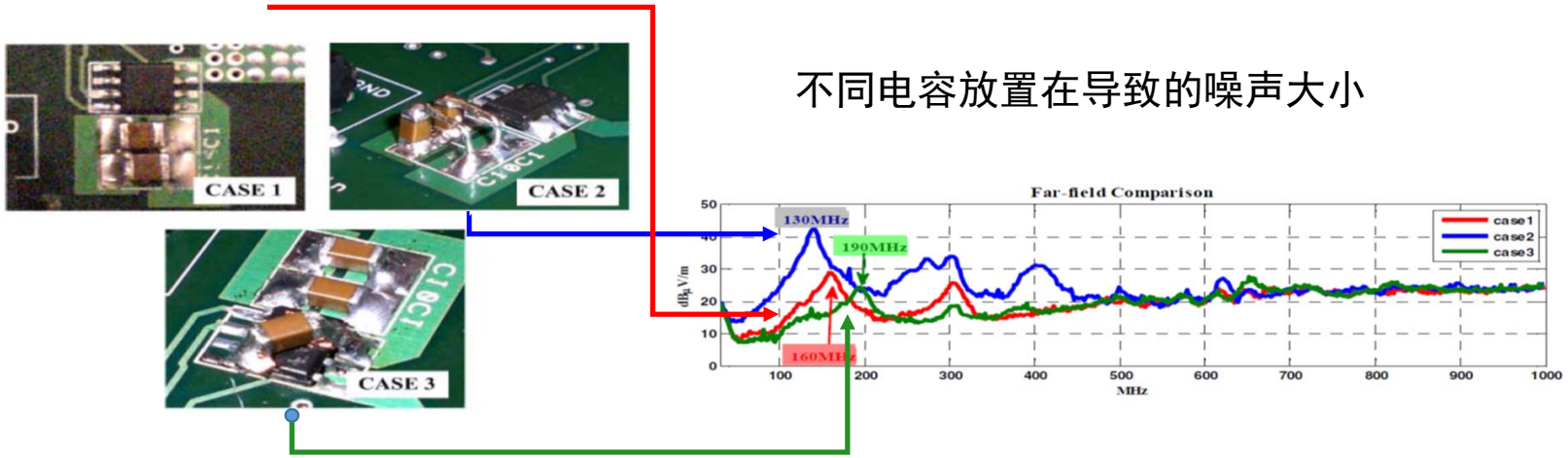


同步buck集成MOSFET，相比较于非同步方案，环路更小，高频电流回路更小，磁场强度更弱

高频电流环路噪声源的抑制

2. 输入电容靠近开关管放置

不同的电容放置方法导致，高频环路的环路大小不一样，环路越小，磁场能量越小



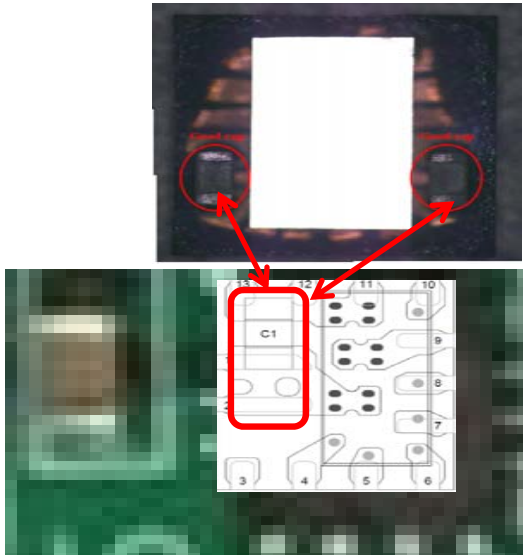
Keong W. Kam, David Pommerenke Cheung-Wei Lam, Robert Steinfeld
EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis

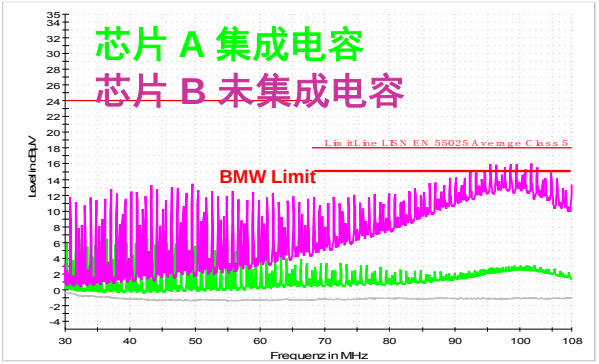
电容要尽可能的靠近开关管，同步buck芯片的输入电容要靠近芯片放置。

高频电流环路噪声源的抑制

3. 芯片内部集成电容

通过芯片内部集成电容的方式，进一步减小电容，MPS在封装以及集成上有先进的工艺和经验





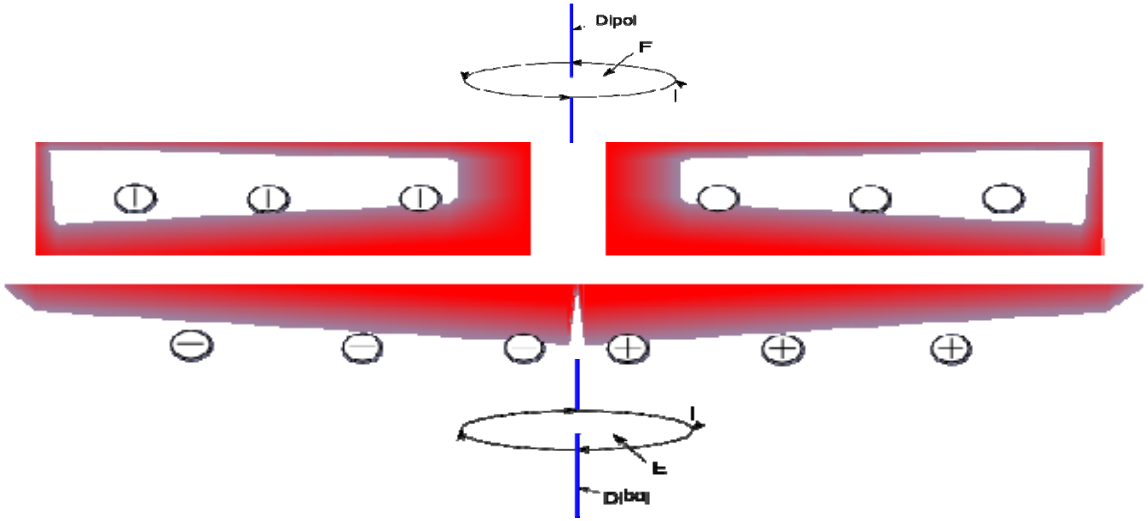
Grey is system noise
Average: 30MHz to 108MHz BW=120kHz

芯片集成电容对EMI有巨大的帮助，可以极大的减小近场辐射的磁场能量，减小输入高频di/dt的环路面积。
对传导和辐射都有很好的改善

高频电流环路噪声源的抑制

4. 高频电流环路底层完整PCB铺铜

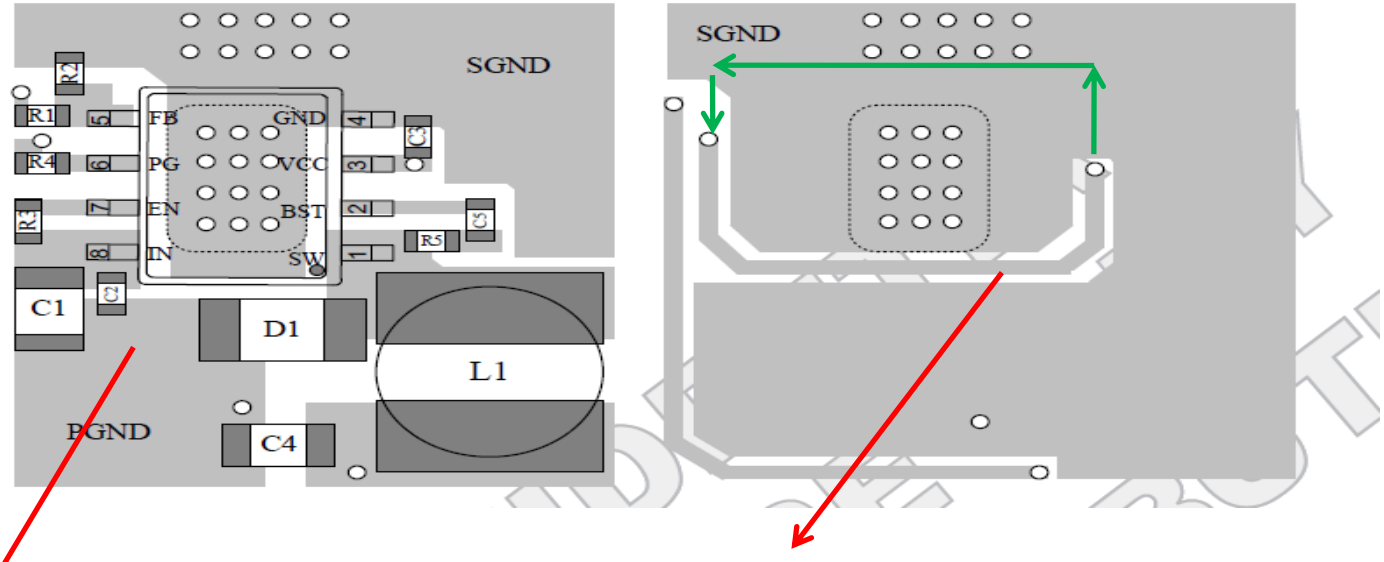
楞次定律：感应电流具有这样的方向，即感应电流的磁场总要阻碍引起感应电流的磁通量的变化。



完整的地平面可以感应出电流，并形成相反的磁场来抵消高频环路带来的磁场。

高频电流环路噪声源的抑制

4. 高频电流环路底层完整PCB铺铜



VIN电容的GND，
这里过孔太少，
需要增加过孔。

这条线路对GND平面切割，导致地平面不完整。

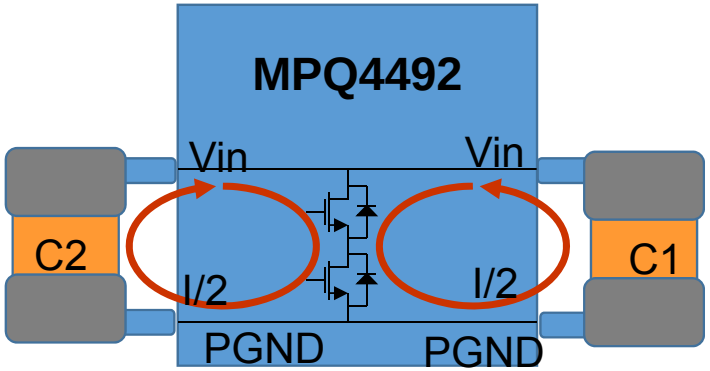
比较好的处理方式是按上图绿色走线。

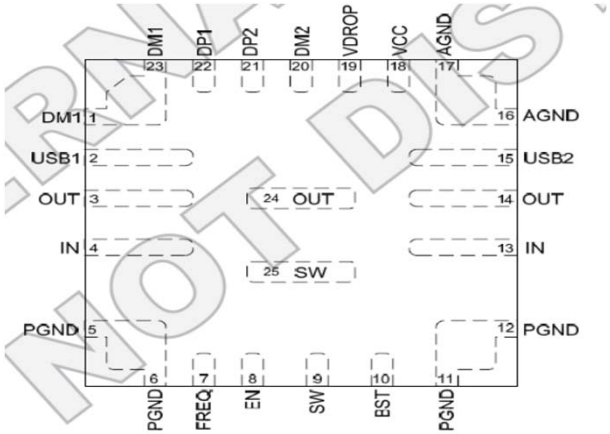
高频电流环路噪声源的抑制

5. 对称放置输入电容抵消磁场

两个输入回路，电流几乎减半，方向相反，外部空间的磁场可以相互抵消

MPQ4492
36V 5A 同步buck芯片
支持双路2.4A，全集成单芯片解决方案，EMI特性好

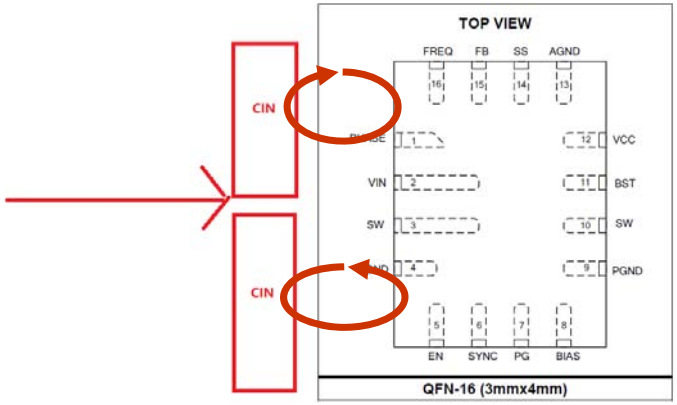


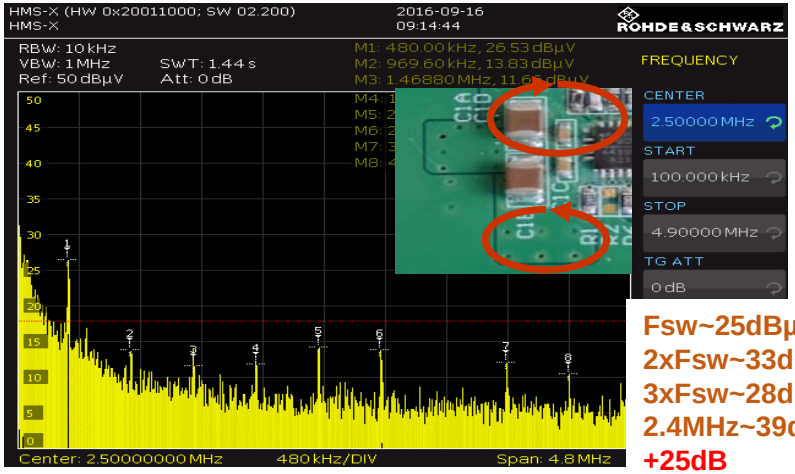


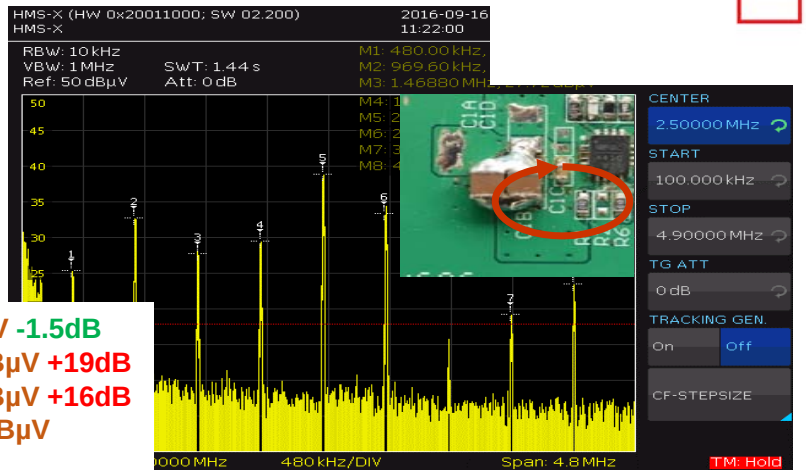
采用对称设计的芯片，两侧都放置输入电容可以很好的减弱磁场的辐射。

高频电流环路噪声源的抑制

5. 对称放置输入电容抵消磁场





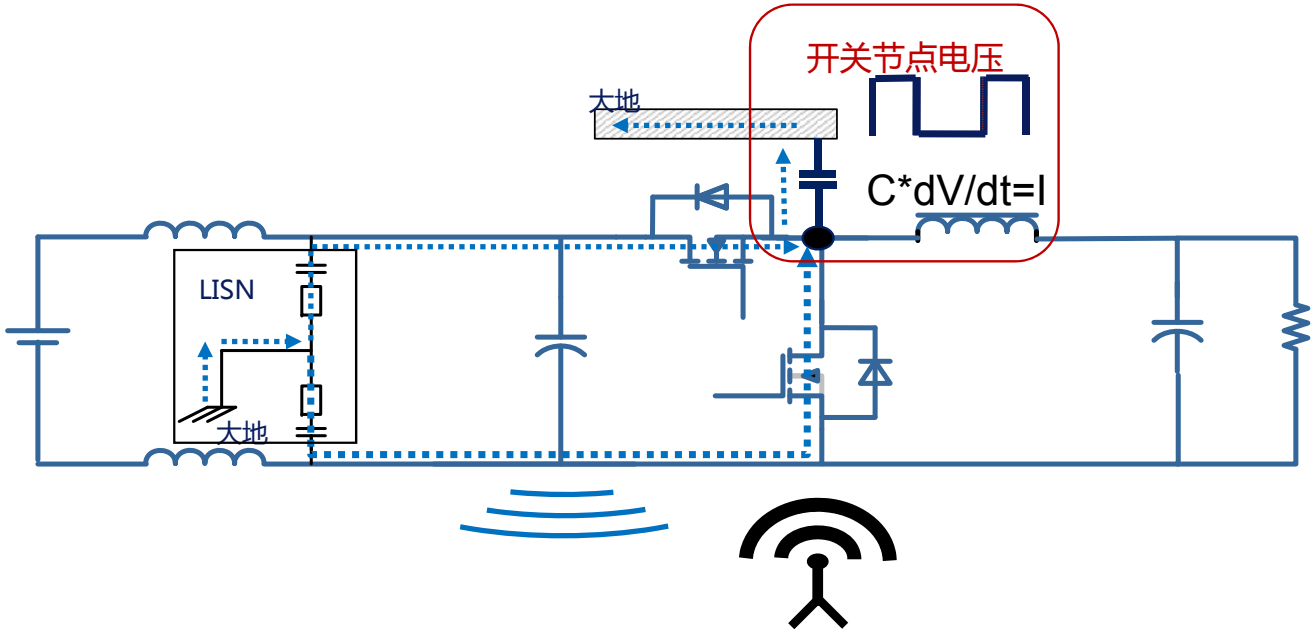


Fsw~25dBµV -1.5dB
2xFsw~33dBµV +19dB
3xFsw~28dBµV +16dB
2.4MHz~39dBµV
+25dB
2.9MHz~33dBµV
+19dB
4.4MHz ~24dBµV
+14dB

采用对称电容设计的电路，磁场抵消后辐射能量减弱

开关节点噪声源的抑制

6: 开关节点噪声源通过耦合电容形成电流



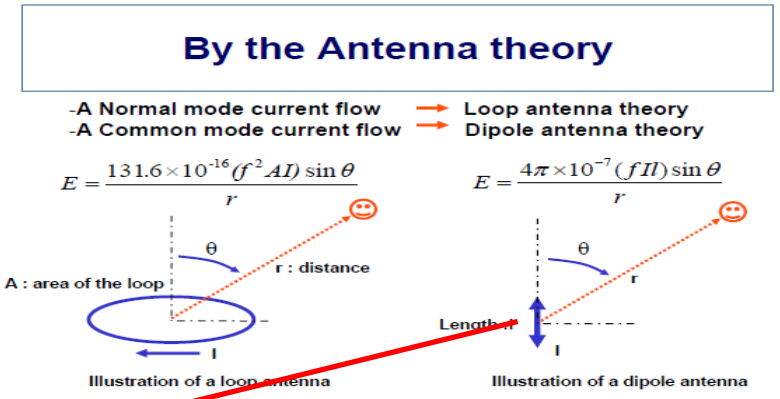
通常会产生共模电流，容易带来辐射干扰

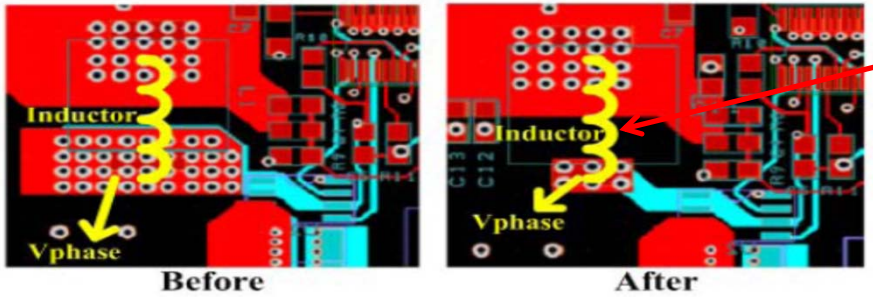
开关节点噪声源的抑制

方法6:

1.减小节点面积，减小等效耦合电容 C的数值。
前提是保证SW散热面积。

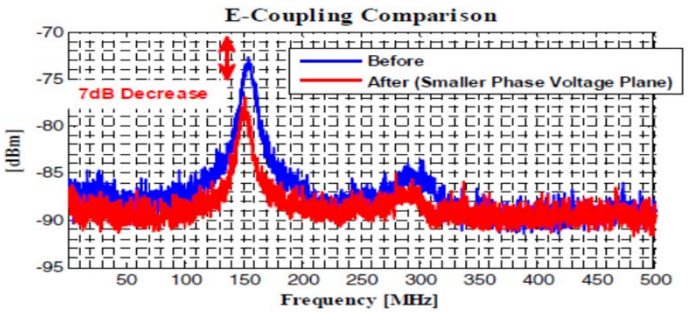
2.增加共模电感抑制共模电流





© Keong W. Kam, David Pommerenke Cheung-Wei Lam, Robert Steinfeld
EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis

减小sw的长度



减小耦合电容和增大共模电感都可以增加共模通路的阻抗，使共模电流下降。

开关节点噪声源的抑制

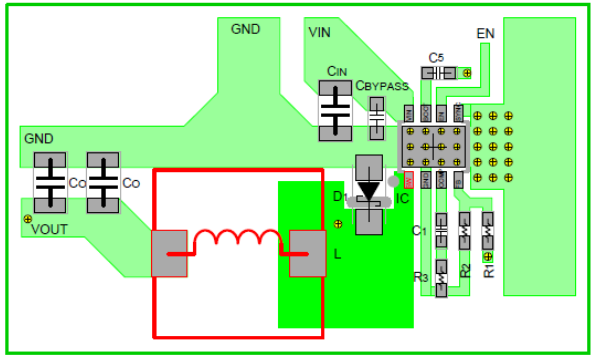


Figure 6-b. Unsuitable wiring to inductor
Unnecessary wide copper area

优化布局与走线

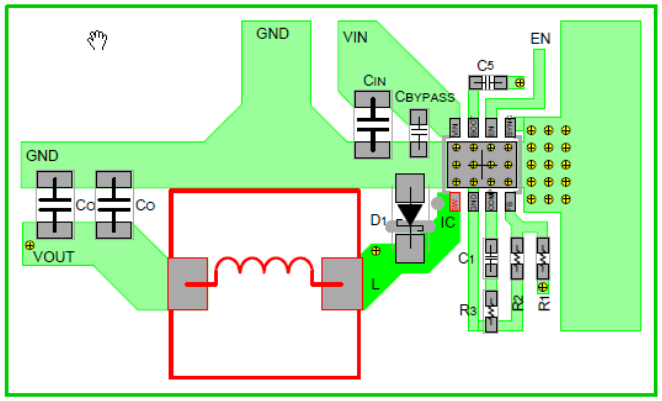


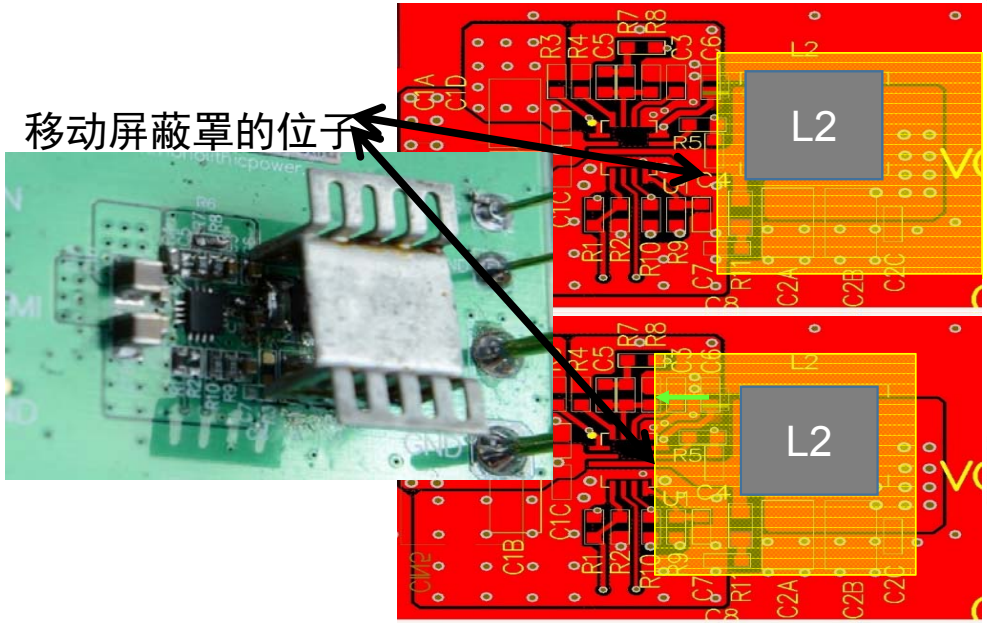
Figure 6-a. Suitable wiring to inductor

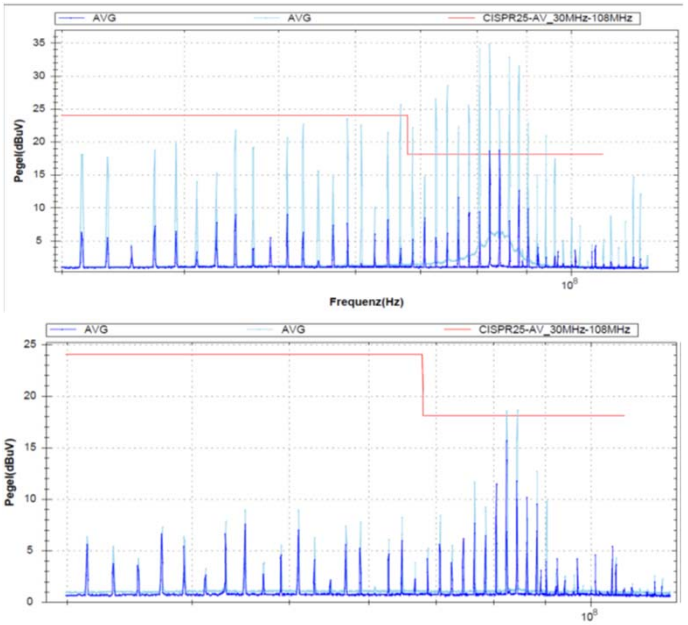
在满足热和承载电流的基础上,
恰当的SW面积与长度是推荐的, 并非SW走线越大越好..

高频电流环路噪声源的抑制

方法　7.屏蔽

移动屏蔽罩的位子





Conducted EMC

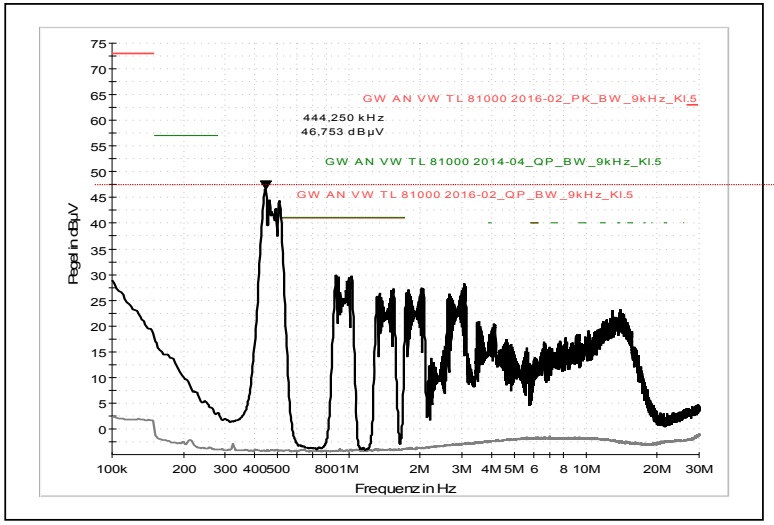
开关节点SW和电感是主要的电压跳变区域，屏蔽主要是针对这两个位置。

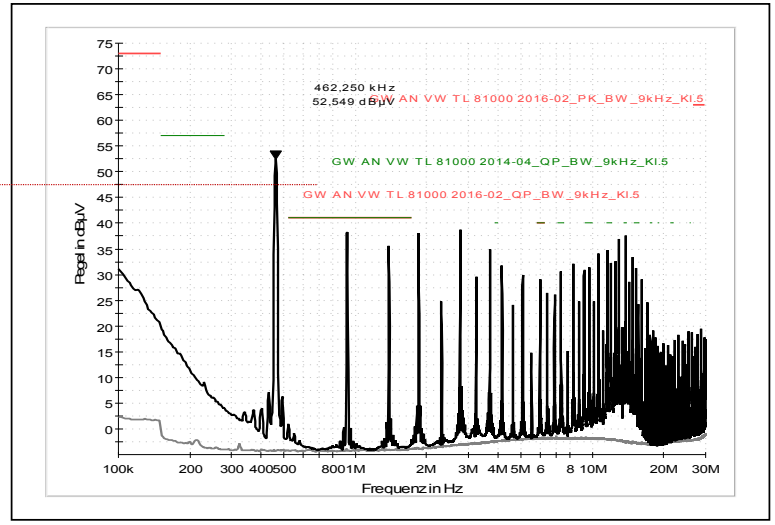
开关电源中用屏蔽电感，会改善EMC性能。

开关节点噪声源的抑制

方法8; 展频可以将能量分散到开关频率附近的频段

CE 100 kHz – 30 MHz – QP - FFT





©Christian Kueck &Jens Hedrich

展频技术可以减低开关频率噪声的集中度，降低低频段的噪声分量。.

目录

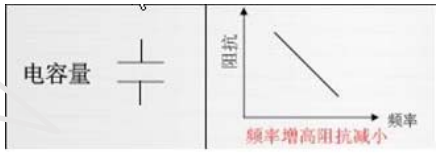
- 1.汽车DCDC芯片EMC的主要内容和趋势
- 2.汽车DCDC芯片EMC特性
- 3.汽车DCDC芯片EMC的设计要点
- 4.汽车DCDC芯片EMC抑制措施
- 5:BUCK 电源的PCB优化设计范例

BUCK PCB layout布局与走线优化

方法9:优化布局与布线,
电容模型，

。

理想状态下，电容阻抗特性如下，当电容真的是电容的时候：
Zc=1/jwc



很不幸： 电容实际模型是下面的：

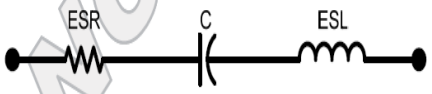
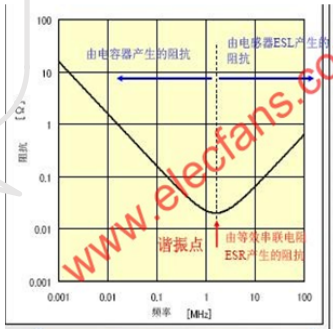


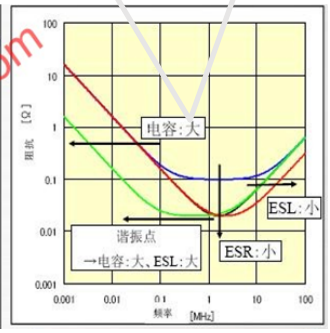
Figure 4 — Equivalent Model of an Actual Capacitor

$$F_R = \frac{1}{2\pi \cdot \sqrt{ESL \cdot C}},$$

高于这个频率点：电容将变成电感。

when
C is larger, the resonant frequency *Fr is lower, and the effective bypass frequency range is narrower*





www.elecfans.com

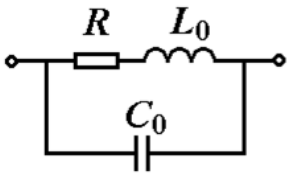
为什么要理解电容模型？为了正确的使用电容

BUCK PCB layout布局与走线优化

方法9:优化布局与布线，
电感模型

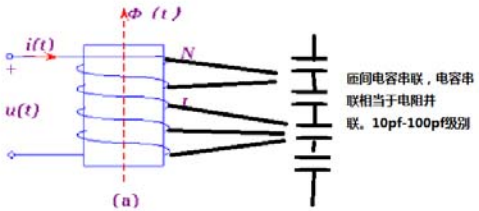
- 为什么电感下面是最好空白？

等效模型



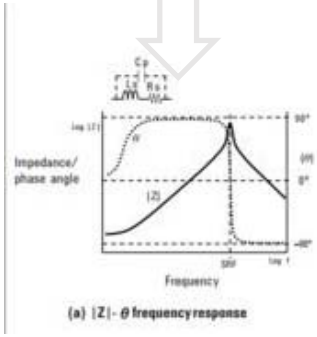
(a)

在一定频率上，电感将变成电容。导线之间的匝间电容将高频信号提供高频通路。



如果电感下方是电感的两个引脚焊盘，靠的很近，又相当于在PCB上放一个小电容，并提供一个高频通路。
所以电感下面是最好是走地线或者空白。

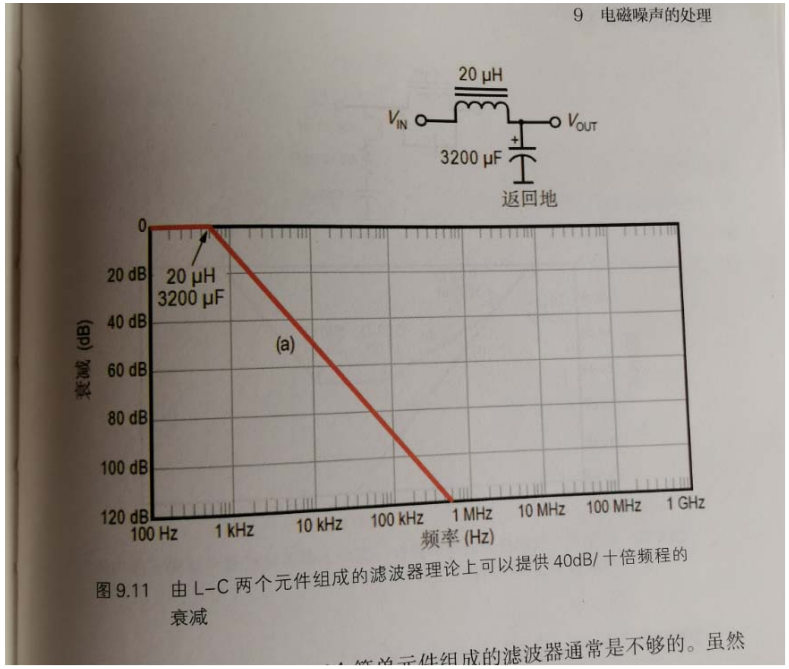
阻抗特性



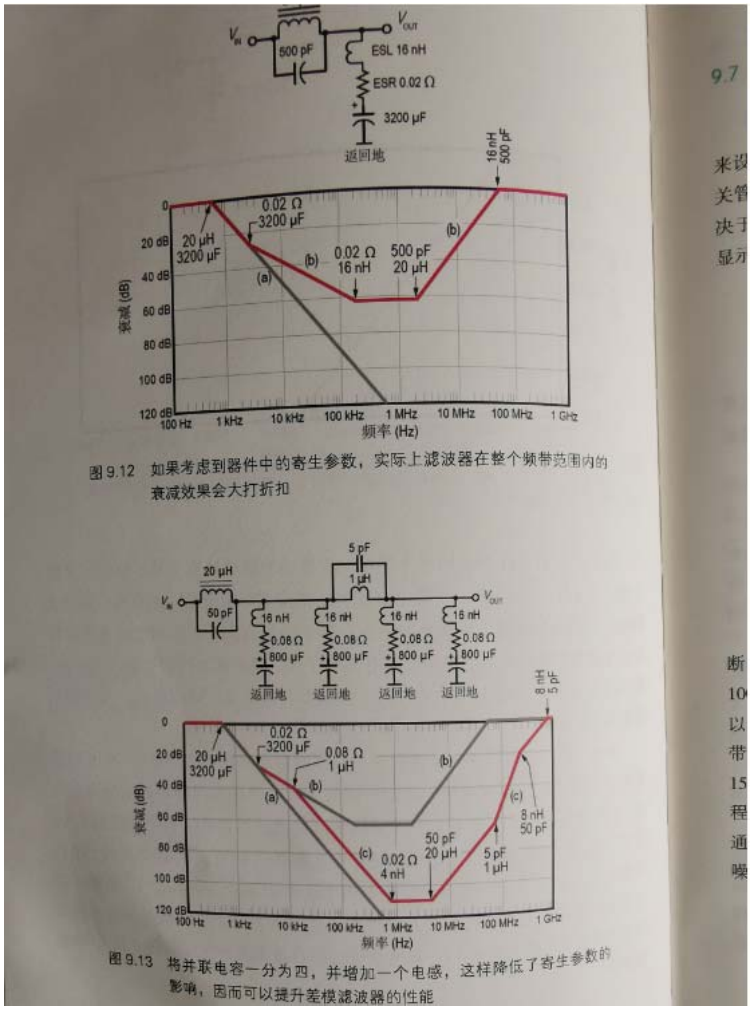
为什么要理解L模型？是为了正确的使用电感。

BUCK PCB layout布局与走线优化

方法9:优化布局与布线，
电感和电容模型对EMC滤波器的影响



理想

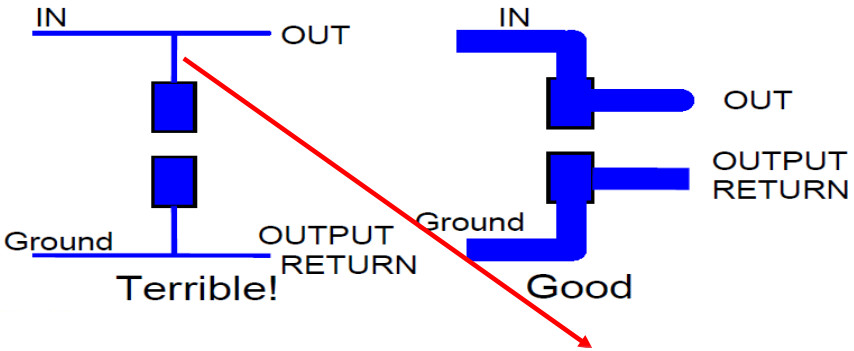


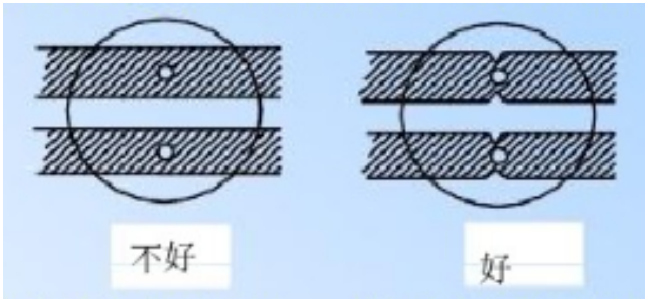
现实

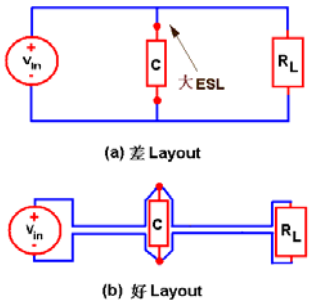
理想模型和现实模型的差异。
假如PCB布局和走线不注意的话， 现实情况会更糟糕。

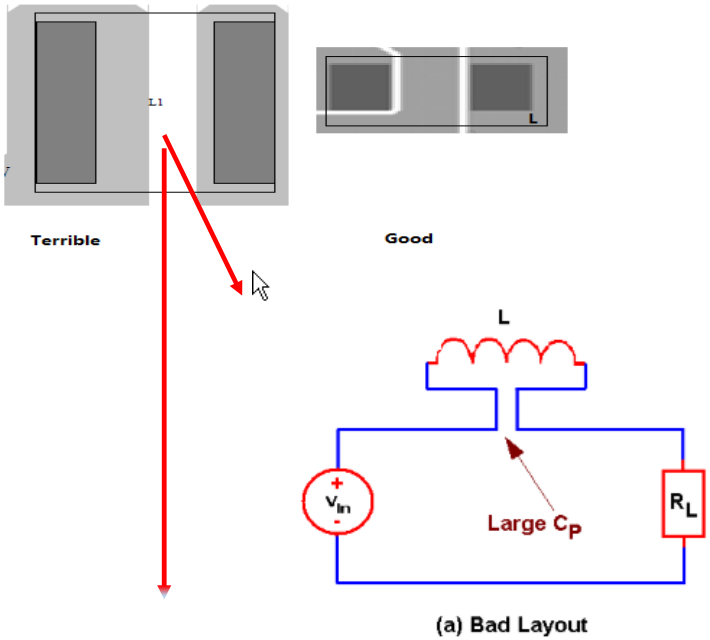
BUCK PCB layout布局与走线优化

方法9:优化布局与布线，
电容和电感的PCB上等效模型









PCB走线之间存在导线寄生的ESR和ESL, 影响电容的高频特性.

焊盘之间存在空间杂散电容, 影响电感的高频特性.

BUCK PCB layout布局与走线优化

方法9:优化布局与布线，
如何走电感下方？

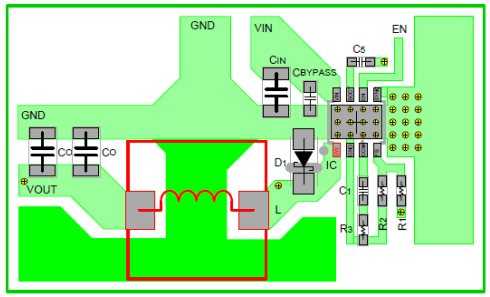


Figure 6-c. Unsuitable wiring directly below inductor

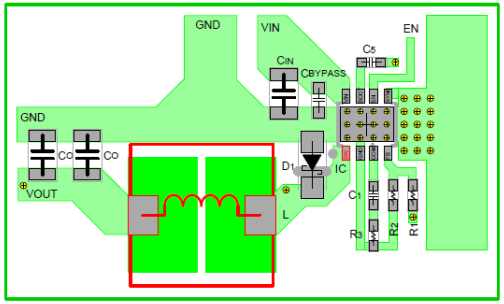


Figure 6-d. Unsuitable wiring between inductor terminals

优化布局与走线

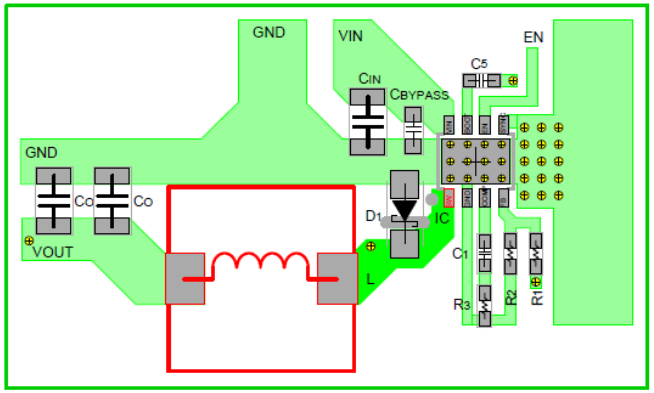
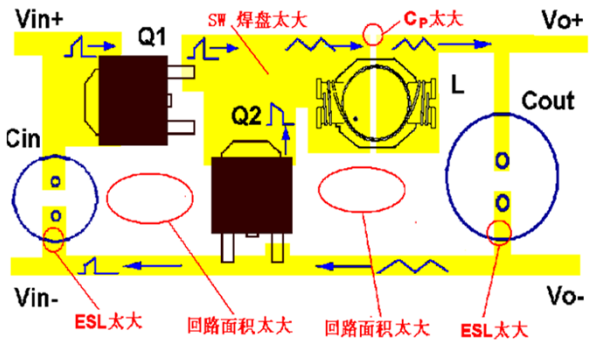
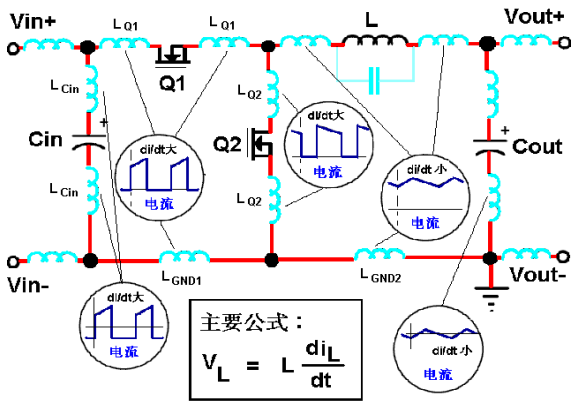


Figure 6-a. Suitable wiring to inductor

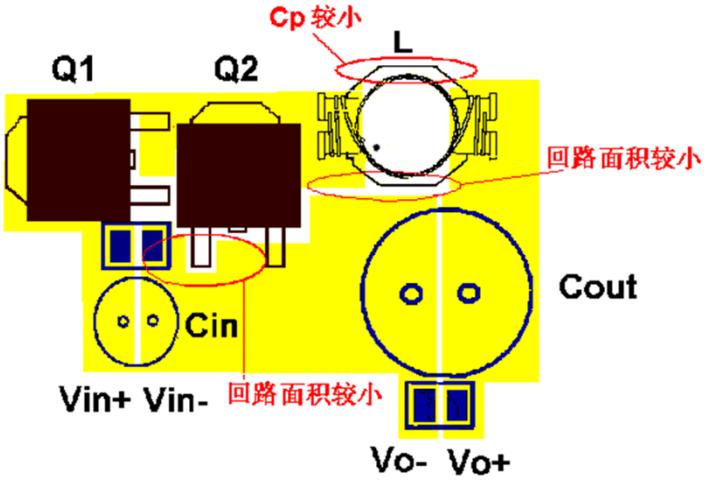
BUCK PCB layout布局与走线优化

方法9:优化布局与布线，
如何整体布局和走线？





优化布局与走线



BUCK PCB layout布局与走线优化

方法9:优化布局与布线，
主要元器件， 输入电容，续流二极管， RC吸收电路，输出电容。

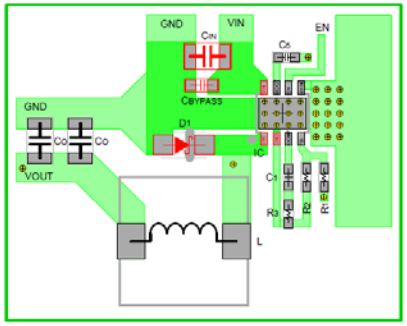


Figure 3-f. Unsuitable layout for diode

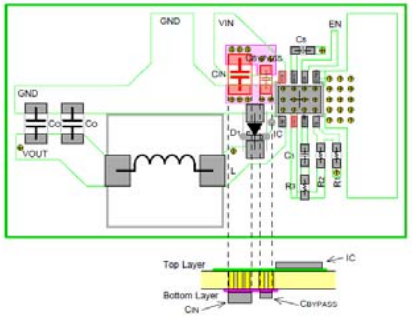


Figure 3-d. Unsuitable layout for input capacitor.
Noise increased by via inductance

优化走线和布局.

1: 缩短Vin pin与 CAP的走线.
2: 缩短Vin GND与CAP GND走线.
3: 缩短续流二极管与IC GND走线.
4:RC snubber 靠近SW与IC GND.

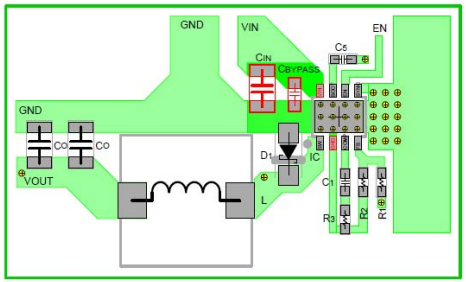


Figure 3-a. Placement of suitable input capacitor

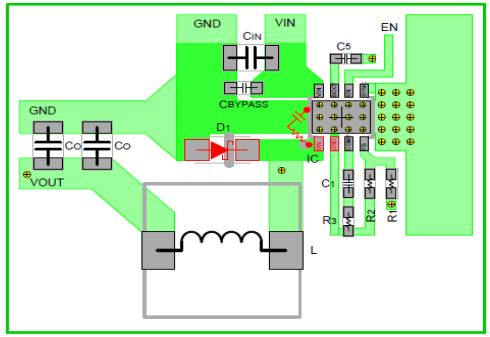
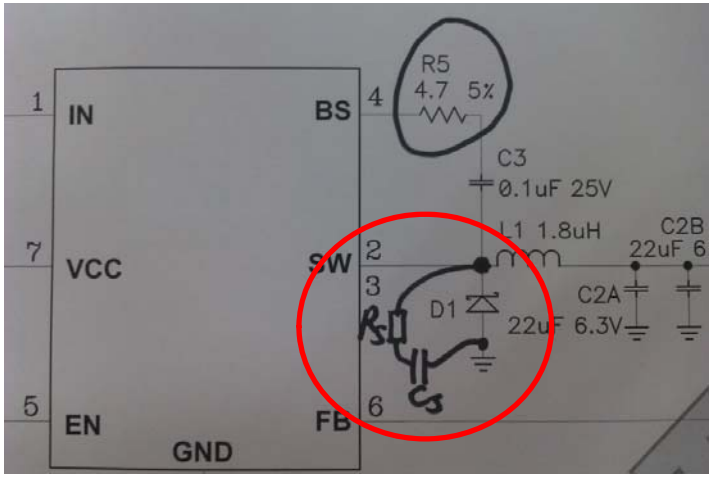
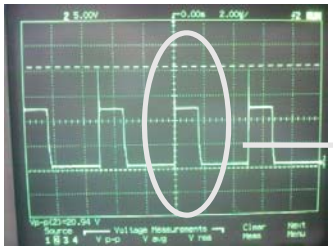


Figure 3-g. Suitable placement of snubber circuit

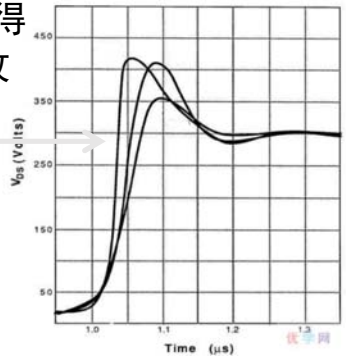
RC snubber 靠近SW与IC GND

方法9:优化布局与布线，
RC吸收电路





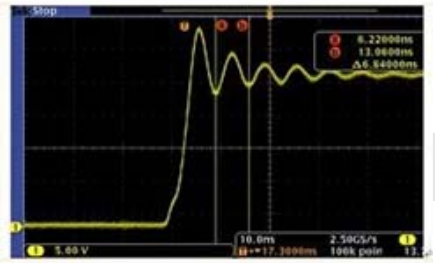
不同的RC，得到不同的吸收效果。



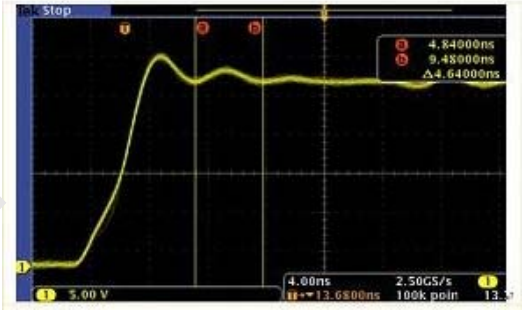
Vsw波形

	Rs	Cs
推荐值	4.7~100Ω	100~1000pF

在SW出对地接个一RC吸收电路，减缓SW处的电压斜率。



加入RC snubber后



BUCK PCB layout布局与走线优化

输入电容距离芯片的远近， 对SW波形和EMC的影响？

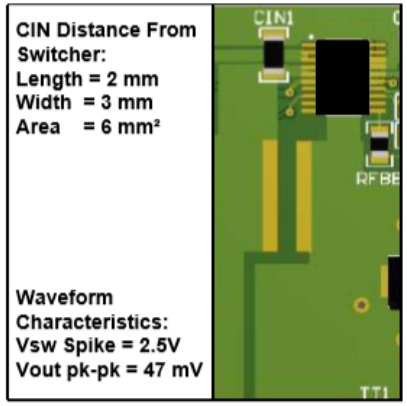


Figure 17. Placement 1

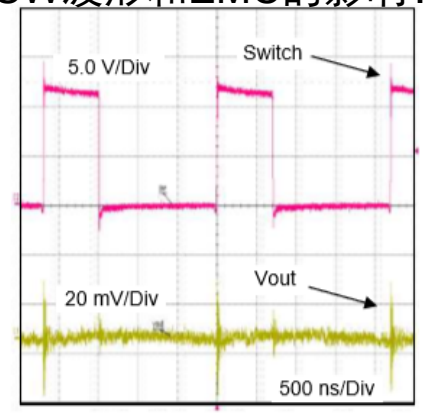


Figure 18. Switching Waveform for Placement 1

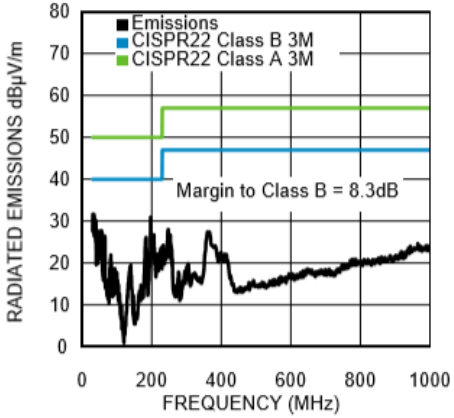


Figure 19. EMI for Placement 1

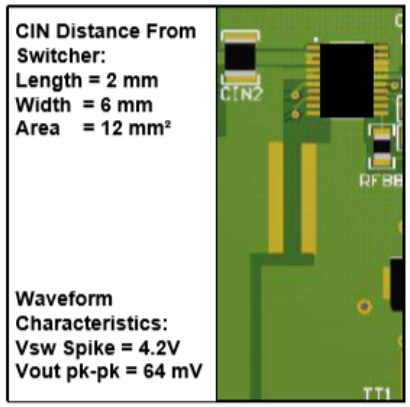


Figure 20. Placement 2

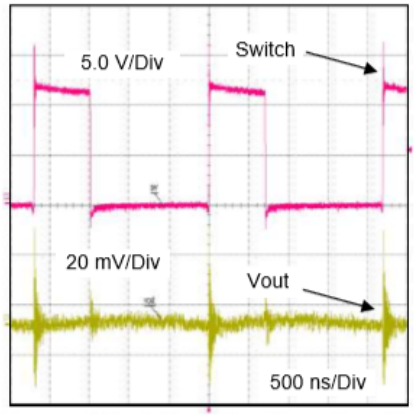


Figure 21. Switching Waveform for

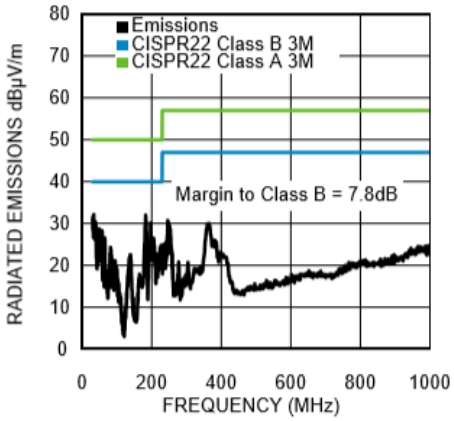


Figure 22. EMI for Placement 2

BUCK PCB layout布局与走线优化

输入电容距离芯片的远近， 对SW波形和EMC的影响？

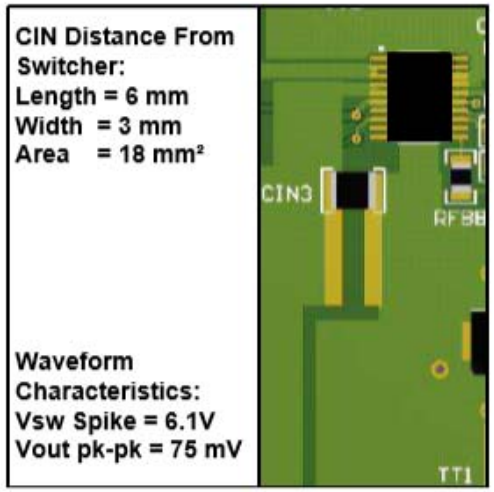


Figure 23. Placement 3

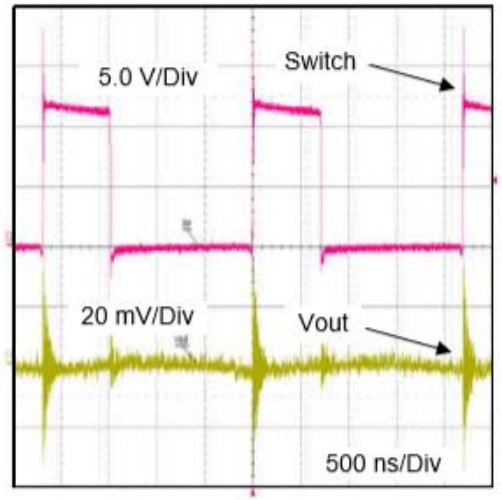


Figure 24. Switching Waveform for Placement 3

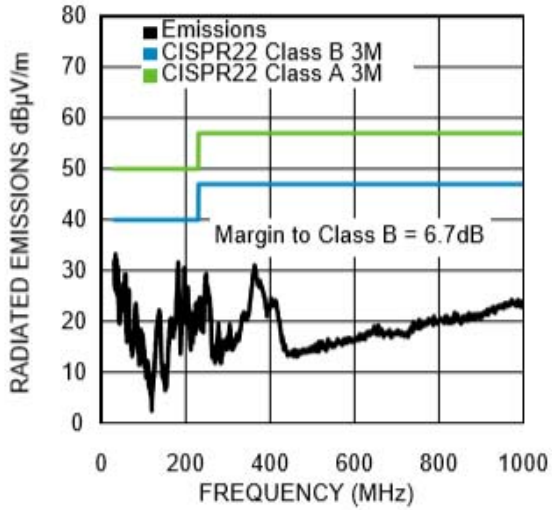


Figure 25. EMI for Placement 3

BUCK PCB layout布局与走线优化

方法9:优化布局与布线
采样点和FB器件

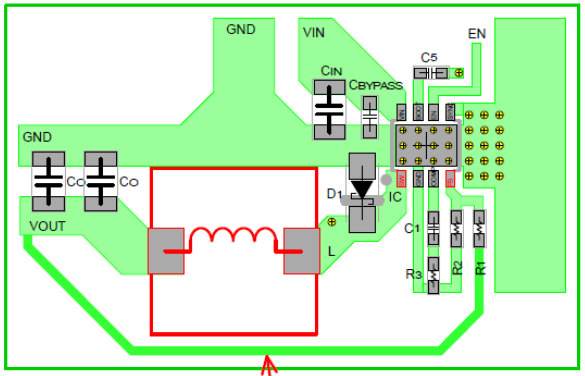


Figure 7-d. Unsuitable feedback route layout
Wiring beside inductor

优化走线和布局.

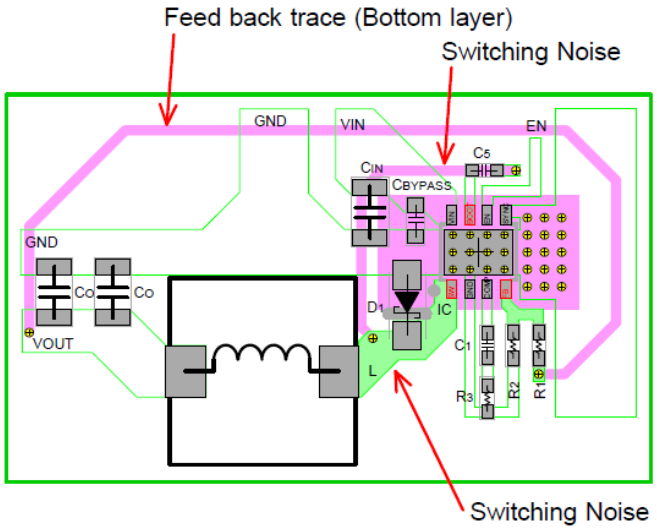
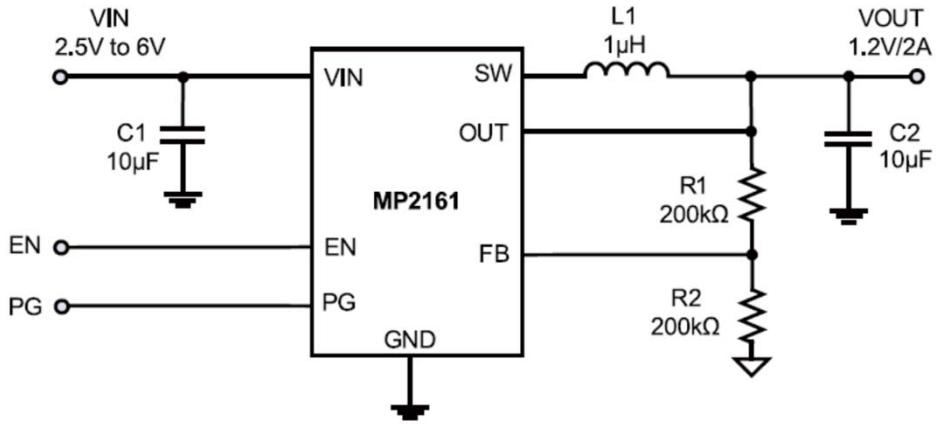


Figure 7-c. Layout example of feedback route.
Wiring through bottom layer

采样点:　　采样点到输出电容的＋
反馈路径：反馈路径要走的干净,有中间GND层的屏蔽与隔离.
　　避免FB途径噪声源 (SW, 电感, BST, 晶振, Vin, VIN_GND,)
　　FB电阻要靠近芯片引脚。

BUCK PCB layout布局与走线优化

方法10: 遇到别扭的 芯片 引脚排布？怎么办？
当pin SW在pin VIN和pin GND中间的时候, 如何处理？



解决方法： 优先VIN和GND， 拉长SW走线。
经管SW走线很细， 但是它也很短， 保证了SW节点很小。

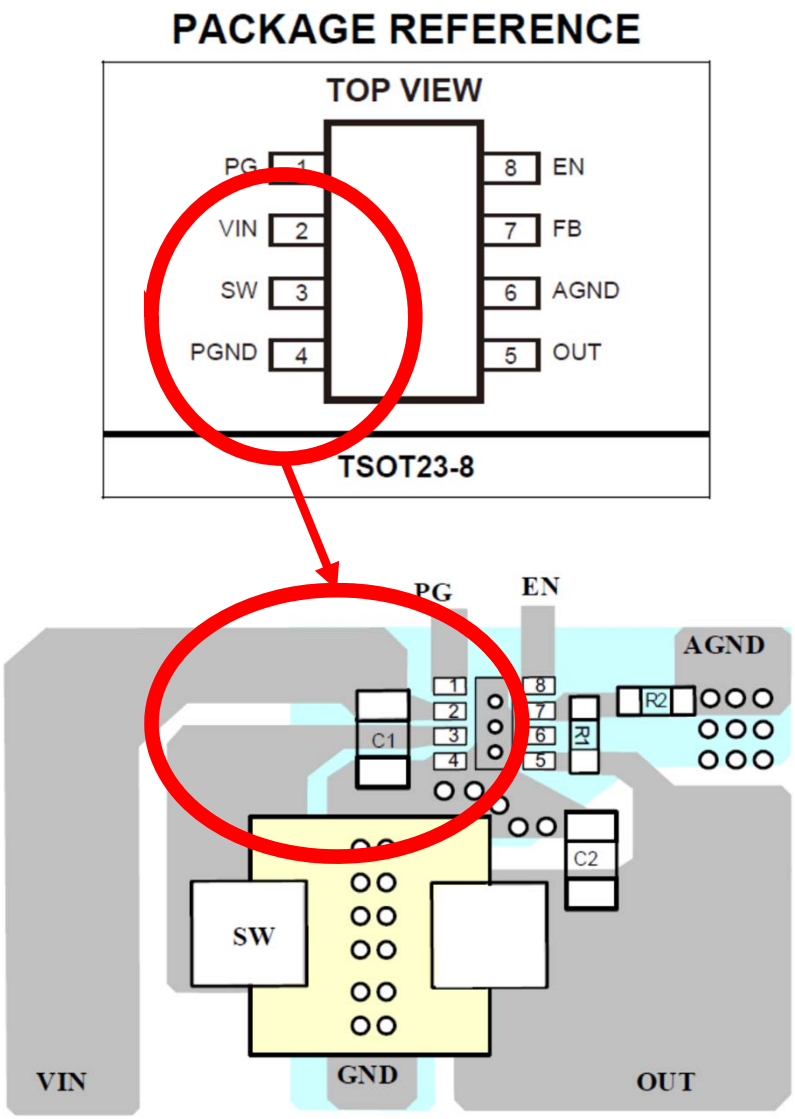
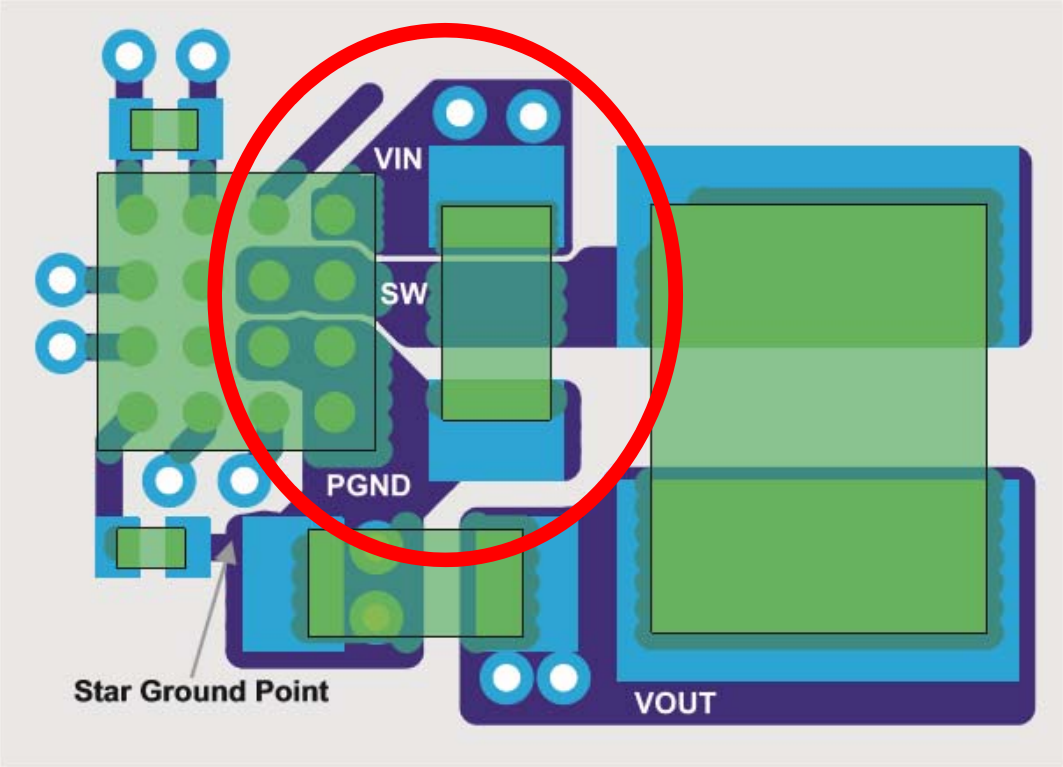


Figure 3: PCB Layout Recommendation

BUCK PCB layout布局与走线优化

方法10: 遇到别扭的 芯片 引脚排布？怎么办？



VIN引脚与GND引脚中间是SW， 如何放置电感和Vin的cap？

如上图的布局会比较好。

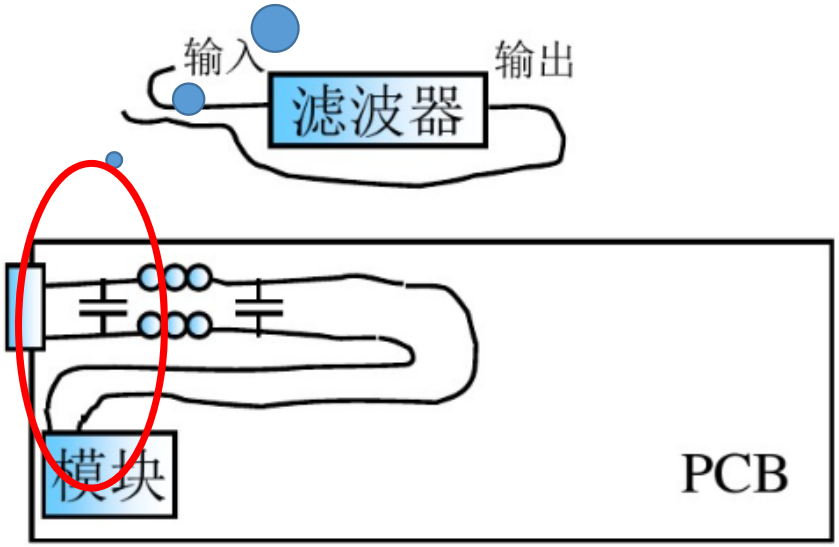
BUCK PCB layout布局与走线优化

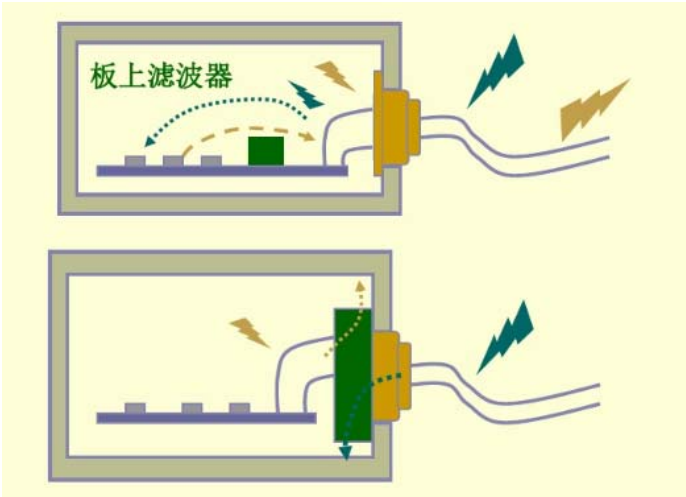
方法11: 滤波器的输入和输出不能靠近，
滤波器对外走线不能过长

图中的L长度有要求；

L避免太长，
假如太长的话，噪
音又耦合出去了。

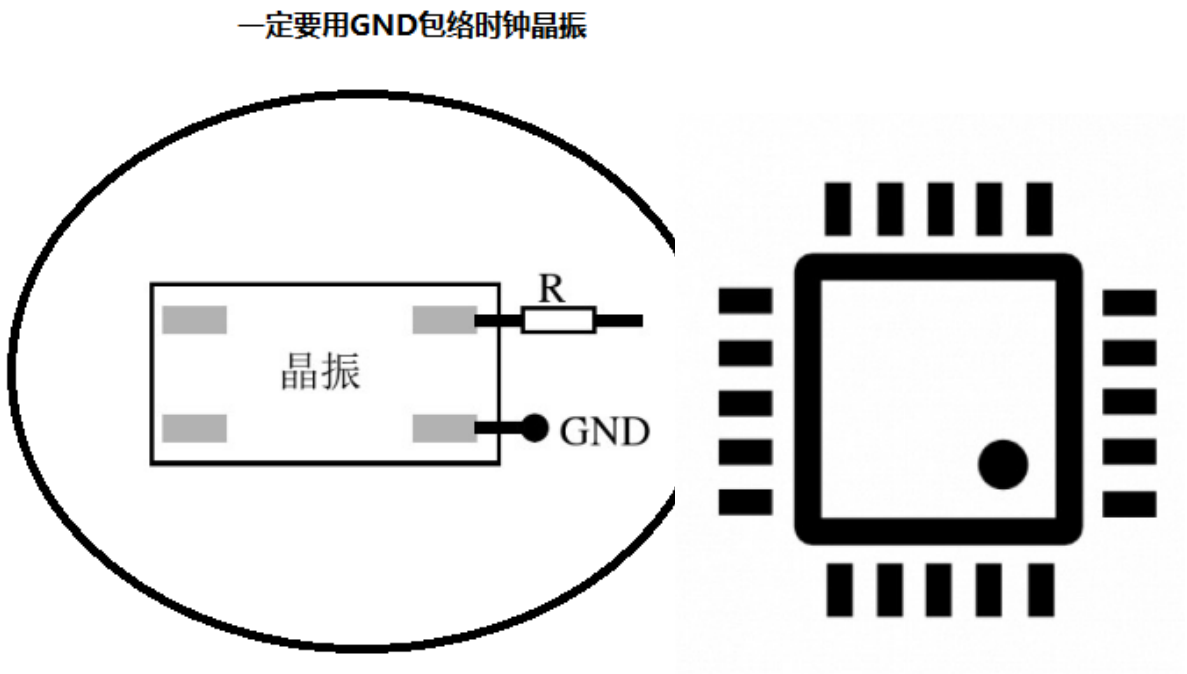
输入和输出挨着，
滤波器起不到应有
的作用





BUCK PCB layout布局与走线优化

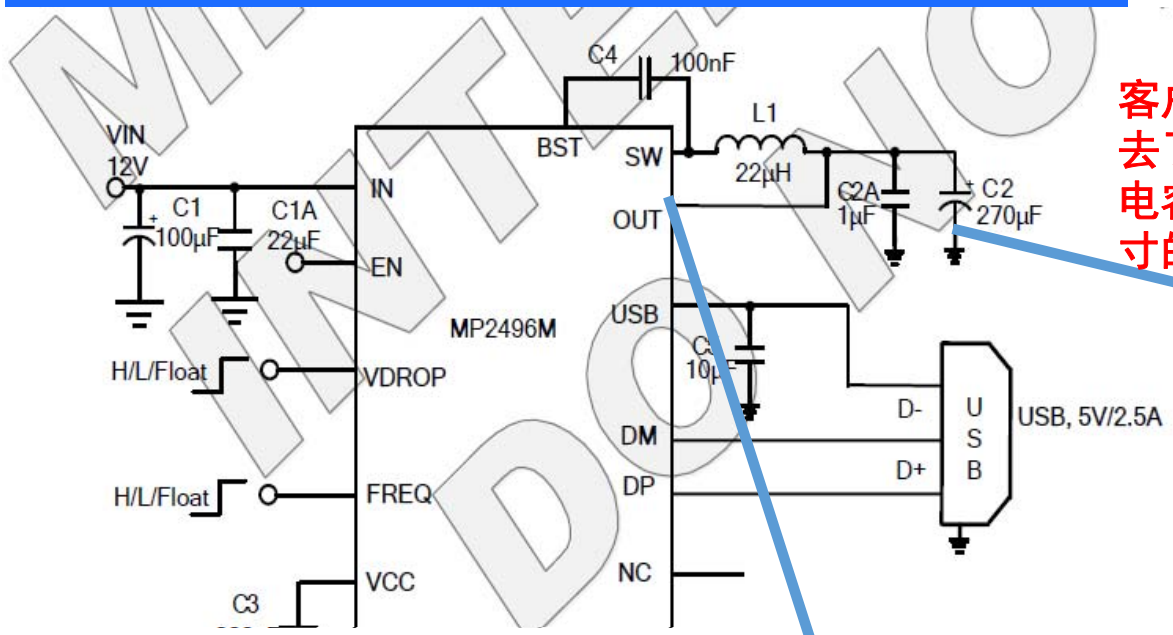
方法12: 屏蔽晶振和时钟



同时靠近负载

几个常见的案例解析

案例分析 1.



客户设计中， 省去了OUT的电解电容。Cost和尺寸的原因。

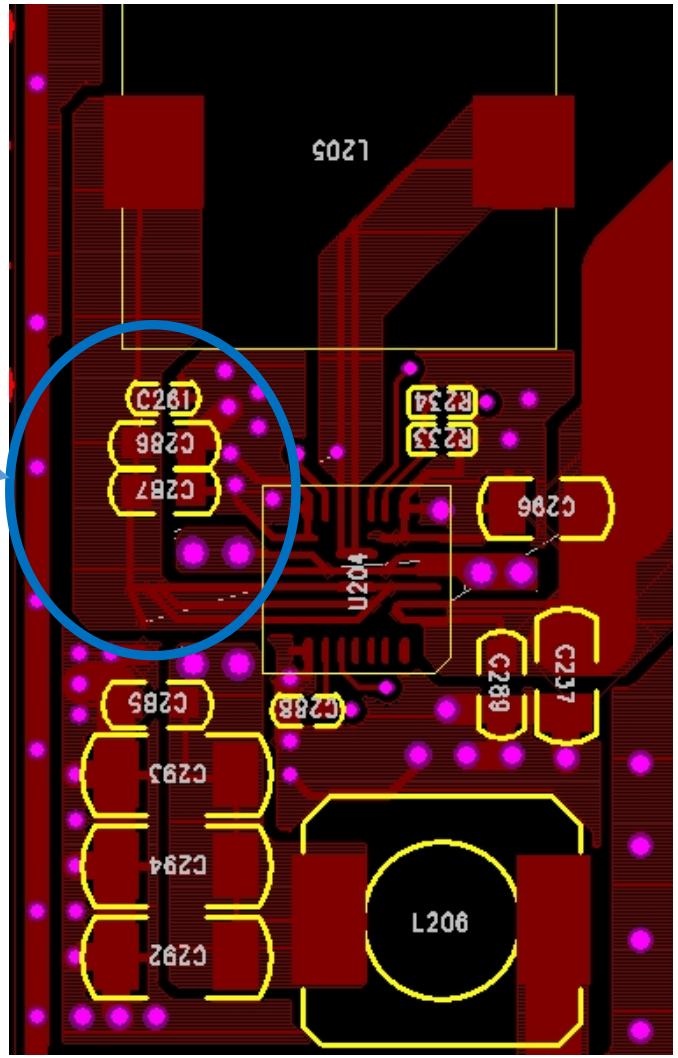


Figure 1

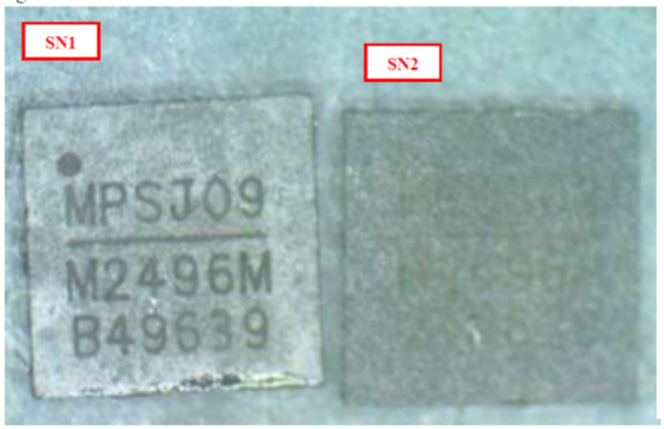
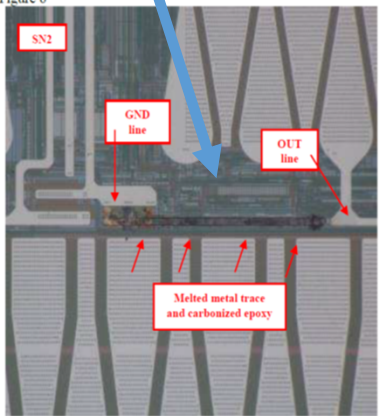


Figure 8

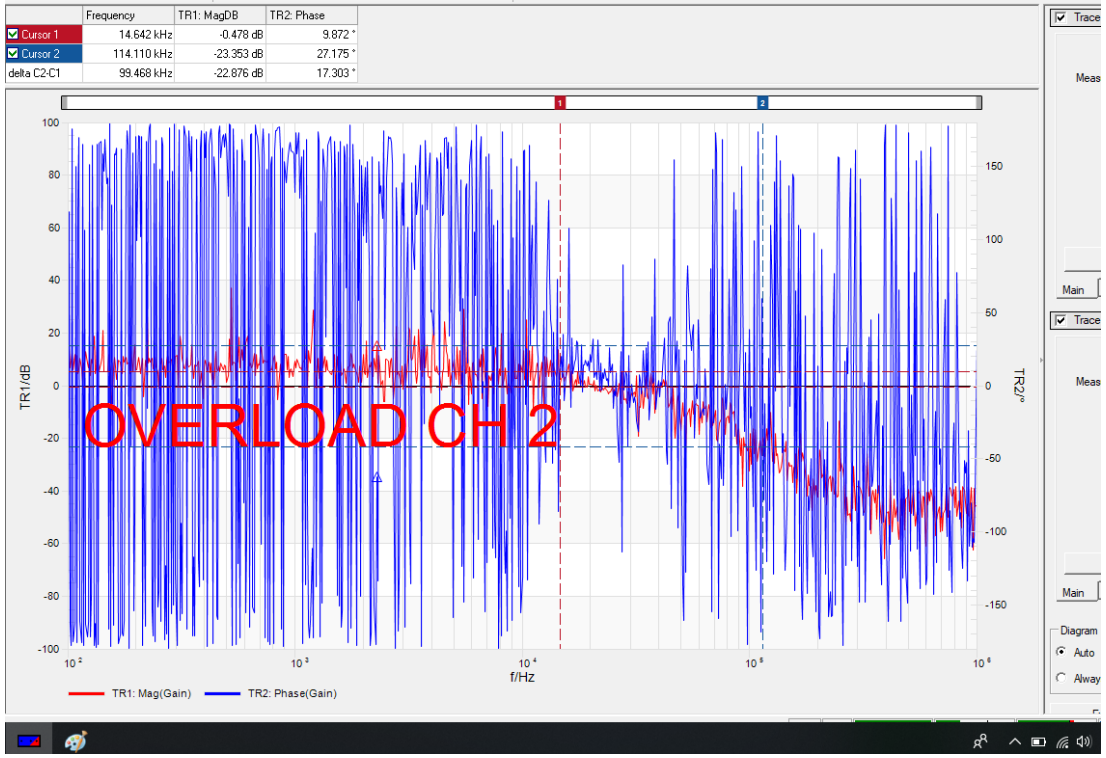


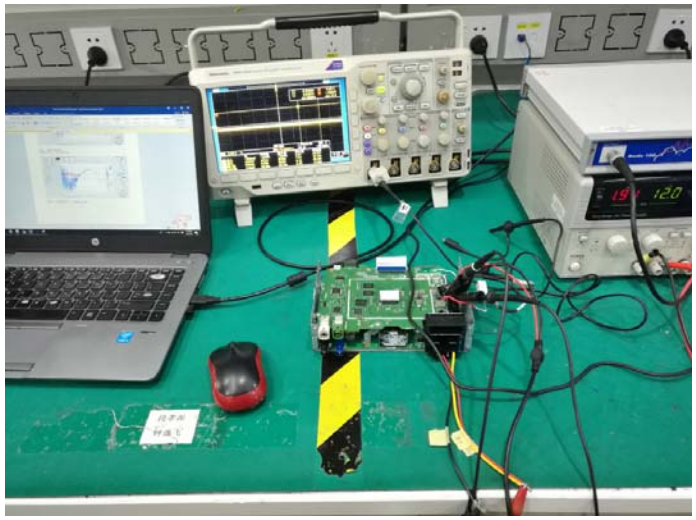
SN 2: De-capsulation
This photo showed carbonized epoxy and melted metal trace under high magnification from figure 7.

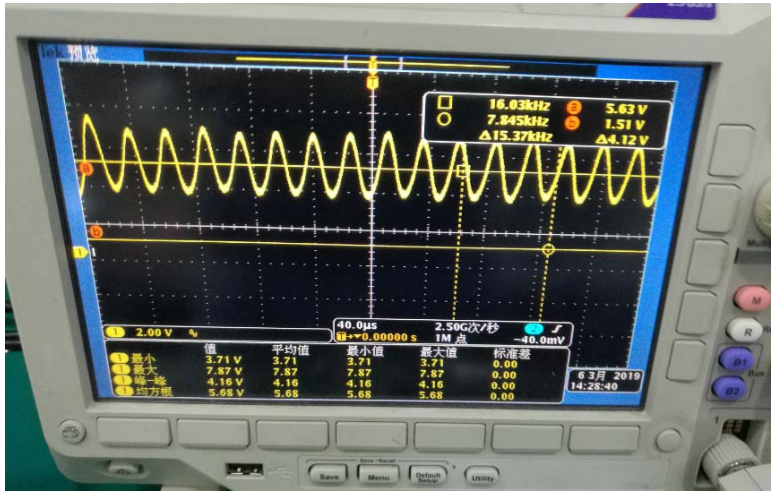
烧坏OUT引脚

案例分析 1

测试1,：原始设计7.5ohm水泥电阻负载输， 出OUT引脚的纹波电压巨大， 无法测试bode图。、
文波电压见附件图形， OUT电压文波太严重， 增大out引脚电容到100uf货220uf后，文波电压消失。



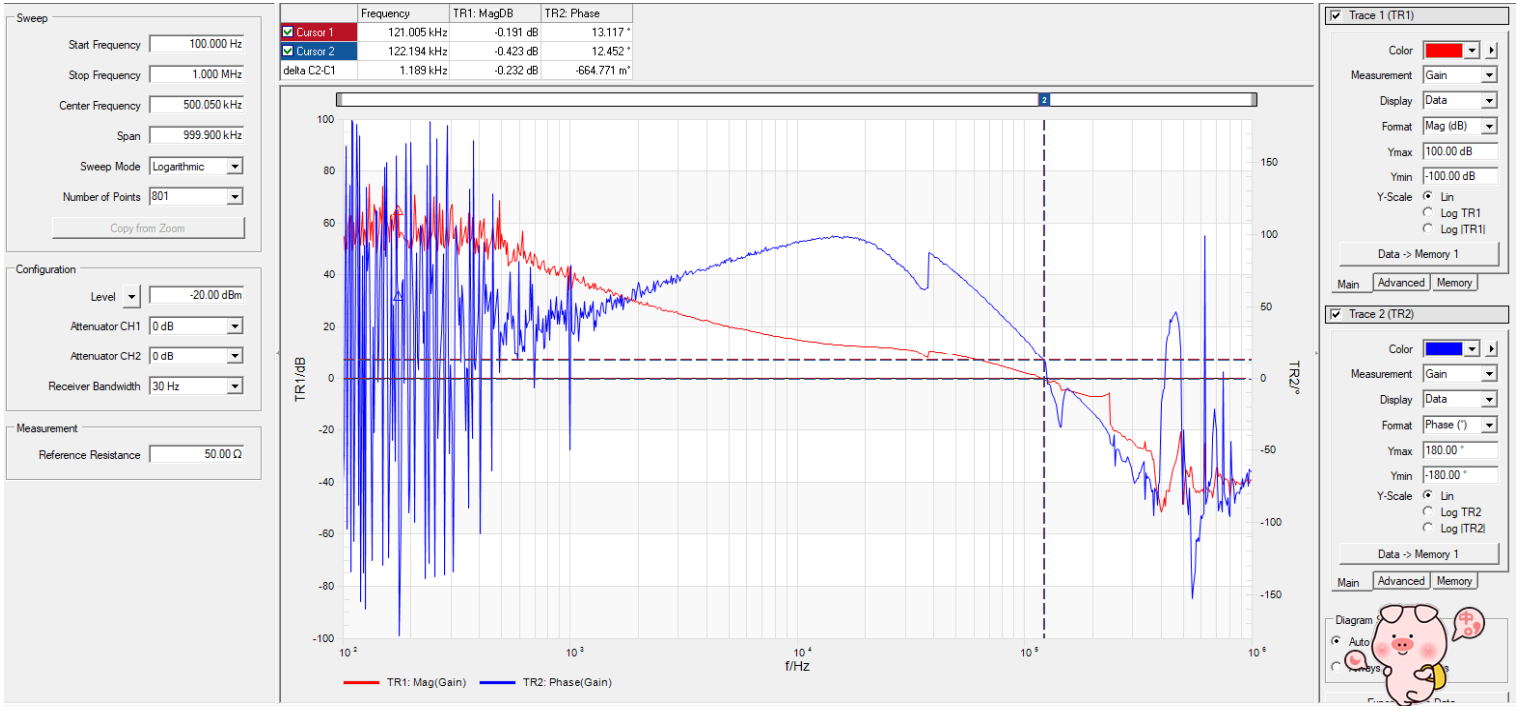




输出5V， 文波电压巨大

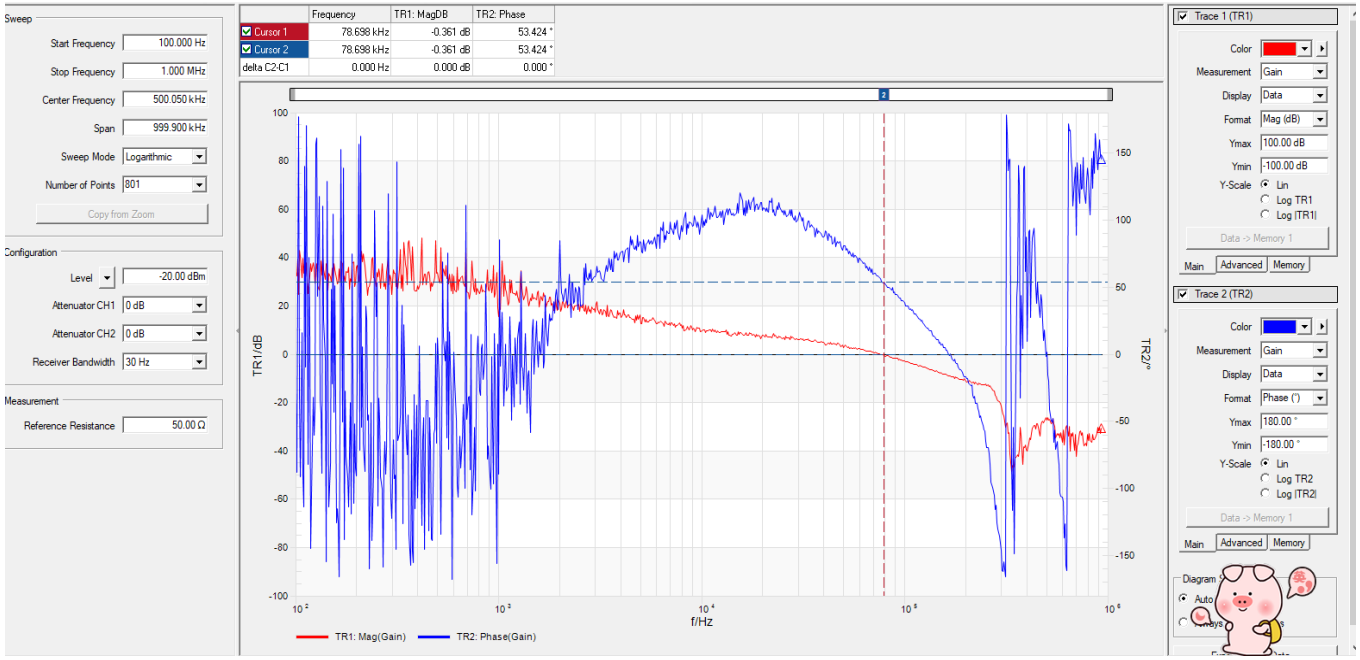
案例分析 1

测试二： 100uf Vout电容， 7.5ohm水泥电阻负载
穿越频率125khz， 相位余量13度。相位余量不足的话，会引起Vout overshoot。



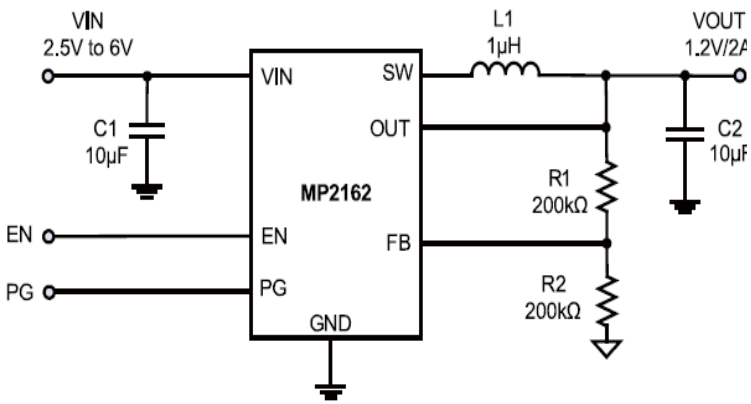
案例分析 1

测试二 200uf Vout电容， 7.5ohm水泥电阻负载穿越频率78khz， 相位余量53度。



案例分析1的结论： 输出电容不可以随意削减。影响环路设计。

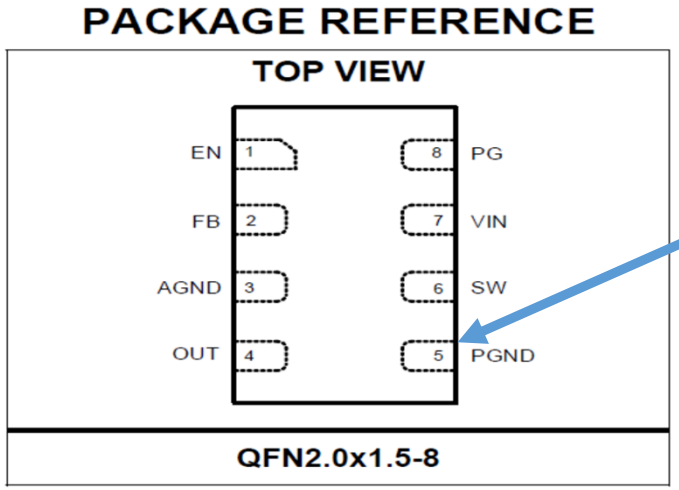
案例分析2

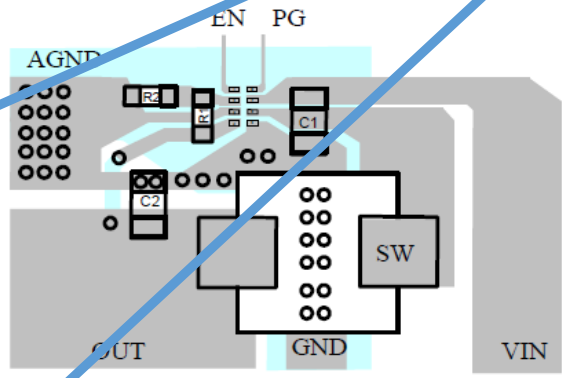


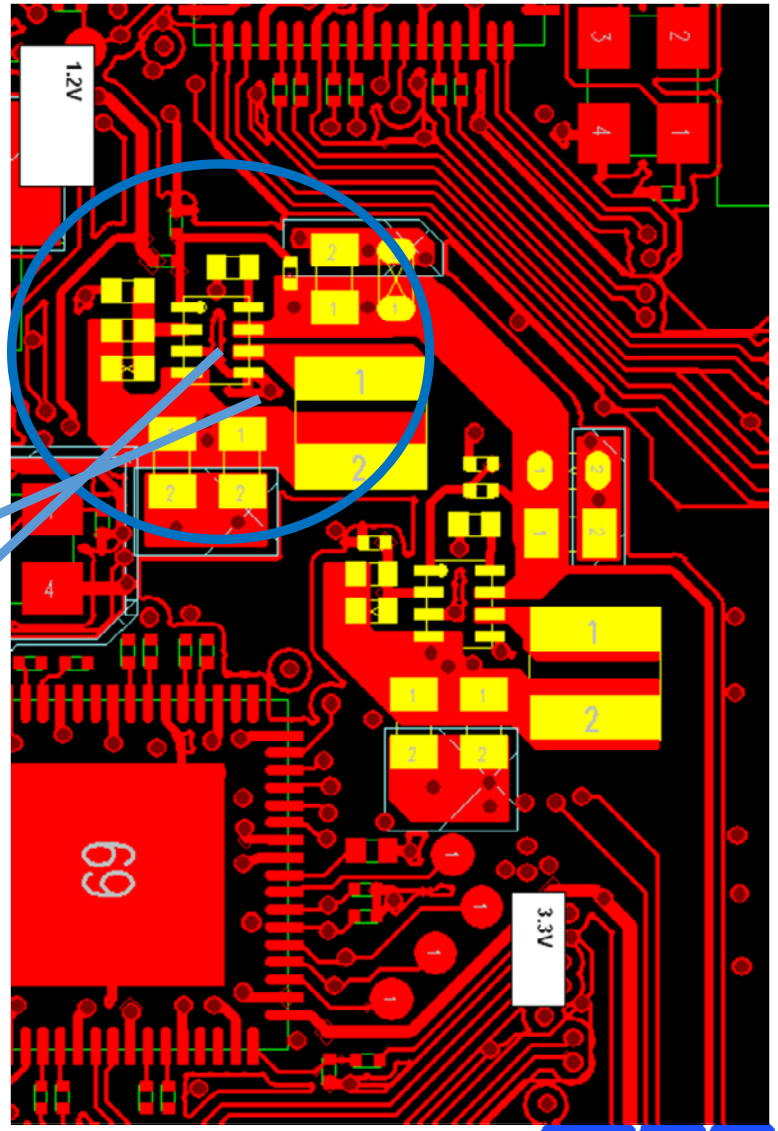
PCB Layout

Proper layout of the switching power supplies is very important, and sometimes critical for proper function. For the high-frequency switching converter, poor layout design can result in poor line or load regulation and stability issues.

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.



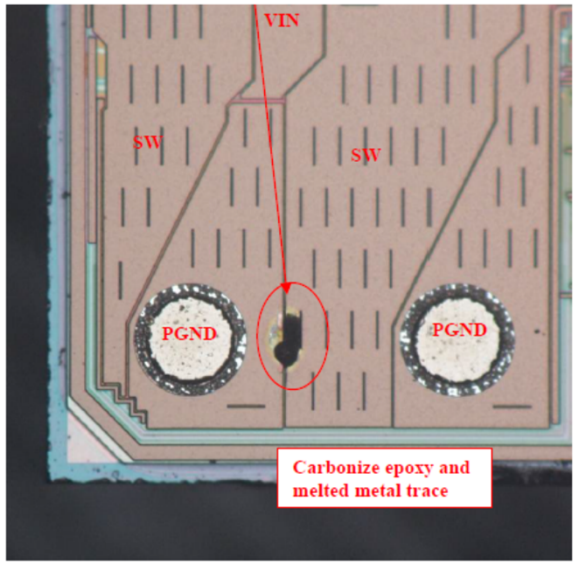




芯片的GND与输出电容的关系， 违反了芯片设计要求。导致芯片烧坏。

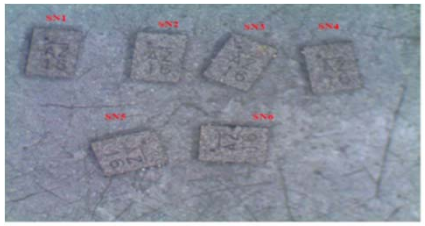
案例分析2

Curve Tracer Results:
SNs 1-6: pin6 (SW) and pin7 (VIN) pin5 (PGND) were electrically shorted together.



SN 1: Decap

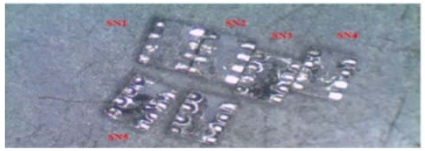
This photo shows carbonized epoxy and melted metal trace at higher magnification from figure 3.



SNs 1-6: Surface inspection

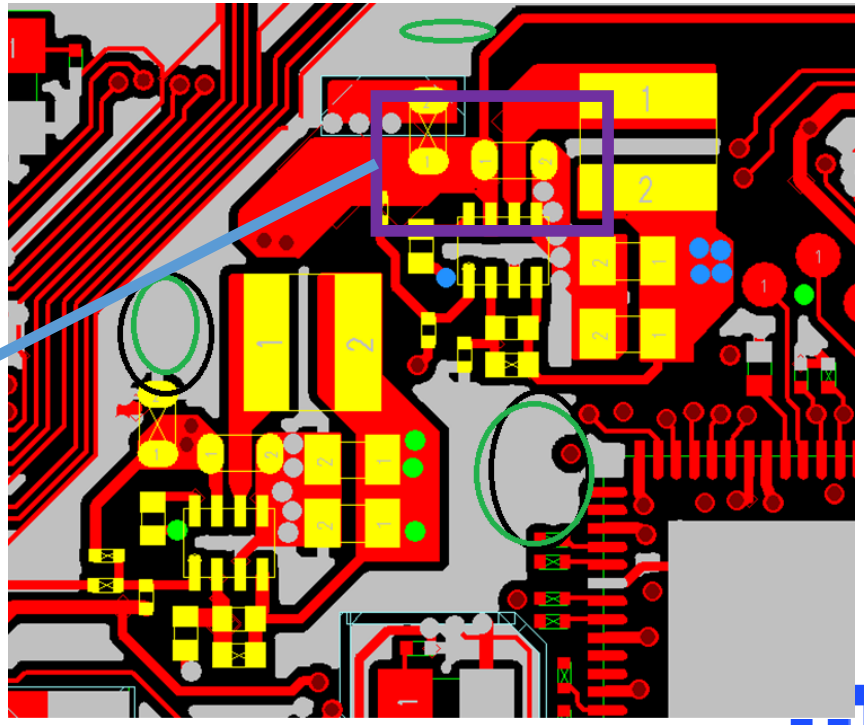
No anomaly was found on package surface.

Figure 2



SNs 1-6: Surface inspection

No anomaly was found on package bottom.



烧坏的芯片样品图片

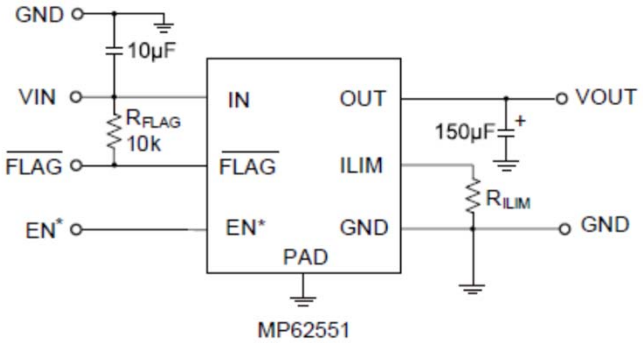
结论：
整改后， 将芯片的GND与vin电容位置摆放好后， 烧片的故障消失。

案例分析 3

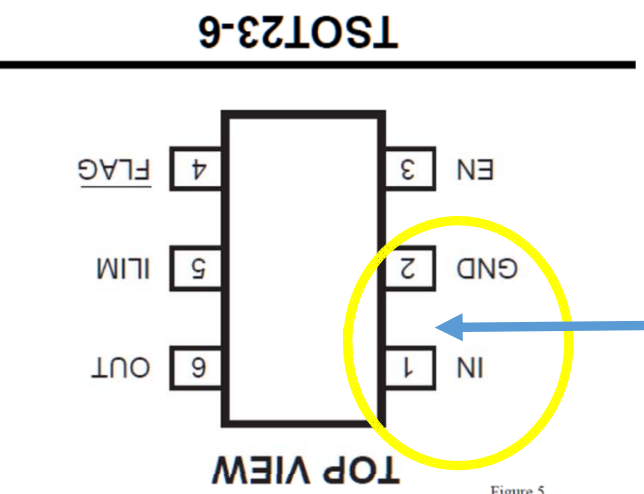
The Future of Analog IC Technology®

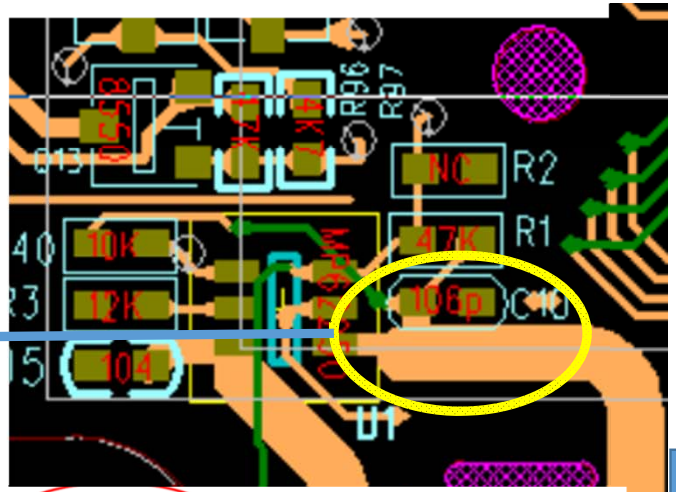
MP62550/MP62551

Precision 60mA-1.7A Programmable Current-Limited Power Distribution Switch



(*EN active low for MP62550)





整改

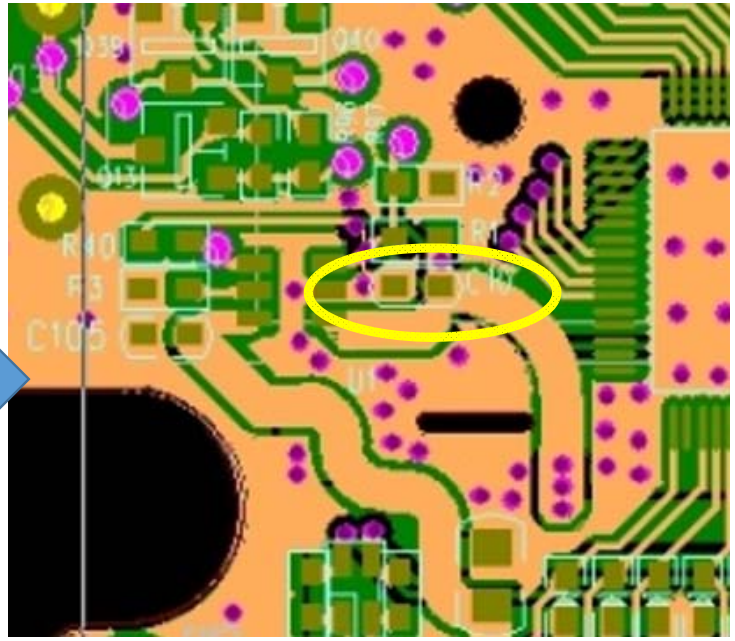


Figure 1

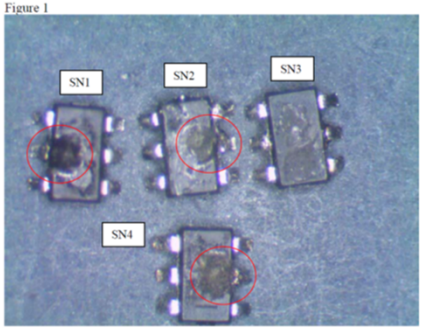
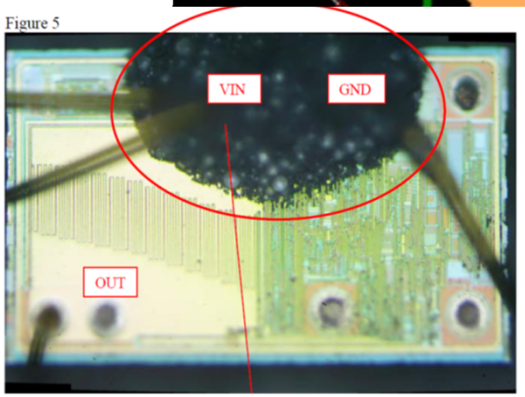


Figure 5



SN 3: De-capsulation
This photo shows carbonized epoxy and melted metal trace on power MOS between VIN and OUT.

整改后，烧坏现象消失

限流芯片， 输入电容的位置导致的烧坏。

参考文献

1: ＜EMI analysis methods for synchronous buck converter EMI root cause analysis＞
David PommerenkeMissouri
Robert Steinfeld
2: ＜PCB layout techniques of BUCK converter＞Rohm
3: ＜ slyt614 ＞ TI
4: ＜ snva638a ＞ TI

END

谢谢