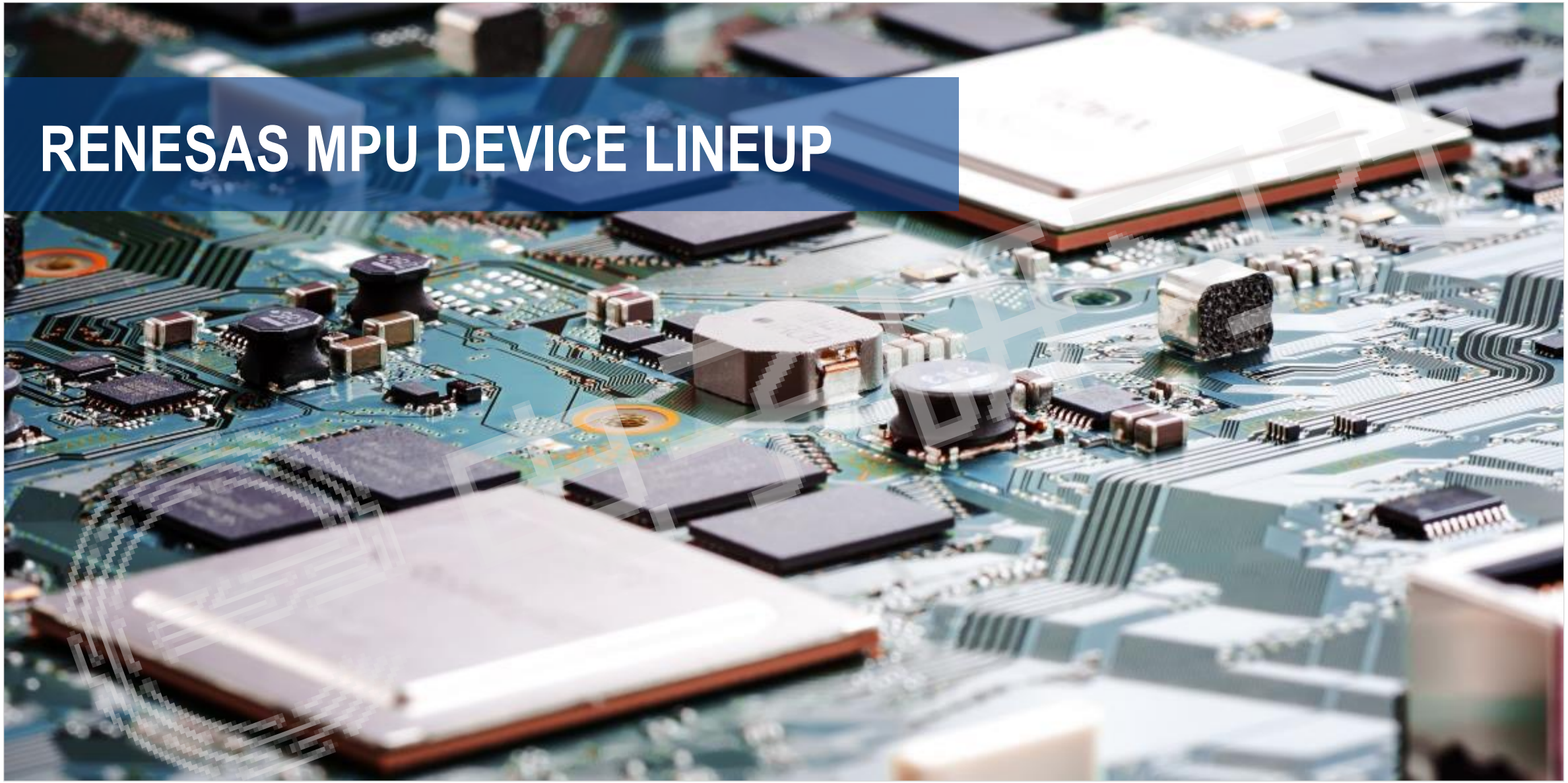
RENESAS MPU DEVICE LINEUP



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RENESAS MPU SERIES

- High performance and Eco-system by ARM core
- Value added IP focusing on specific market needs
- Newly release RZ/V for Vision-AI market with AI-Accelerator

RZ/A Series

Display Systems
Human Machine Interface
Computer Vision
embedded-AI

"Application"

"Graphics"

RZ/G Series

High Performance
High Reliability
3D Graphics
FHD and UHD Video
Verified Linux Package

RZ/V Series

Vision AI with DRP
Display Systems
Human Machine Interface
Robotics

"Vision + AI"

RZ/T Series

Precision Real-Time Motor
and Drive Control
Industrial Ethernet

"Real Time"

"Network"

RZ/N Series

Industrial Network Gateway
Multi Protocol

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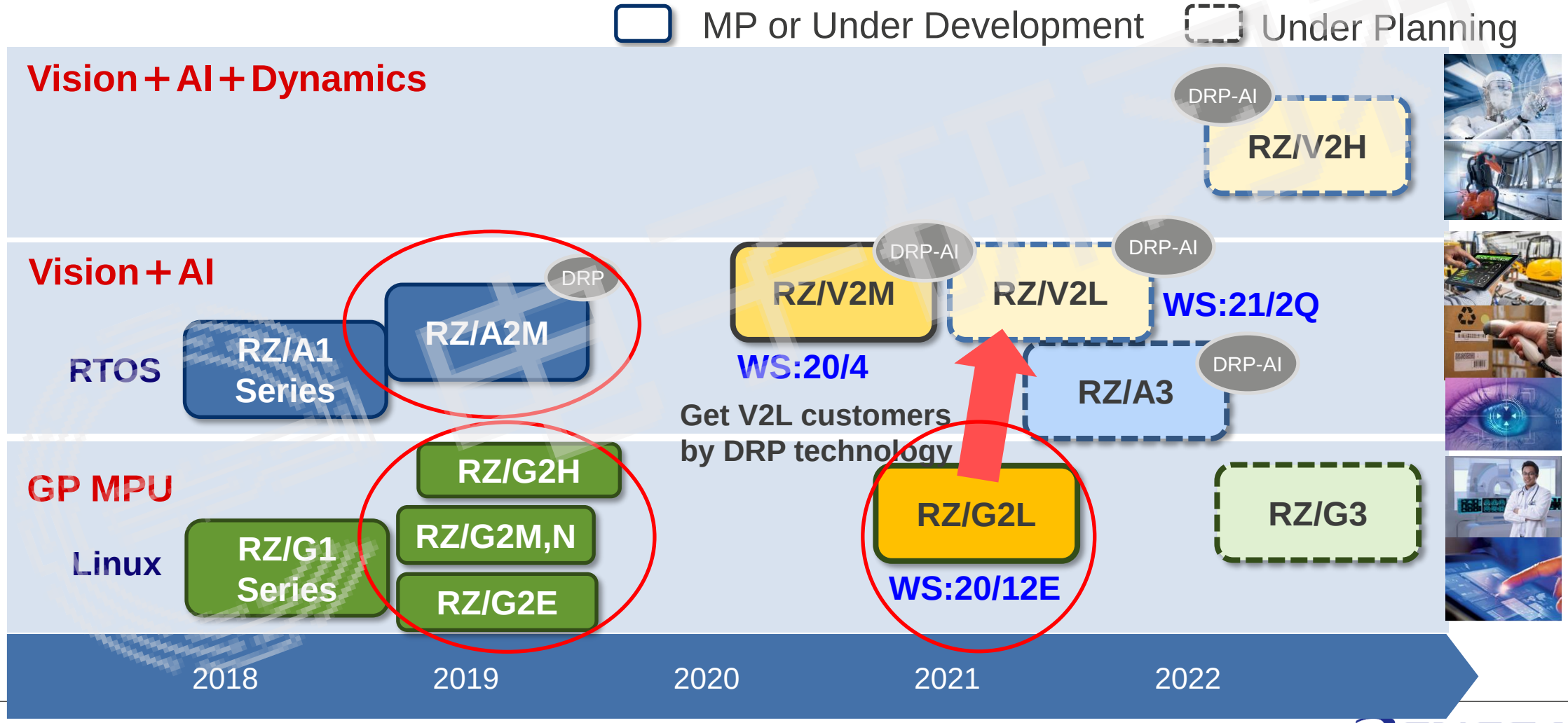
EPBD PRODUCT ROADMAP UPDATE (RZ MPU)

- RZ/G2 & A2M are focused, and G2L for HMI 5~7$ market will be added in FY20.
- Let's visit customers with V2M AI Demo.



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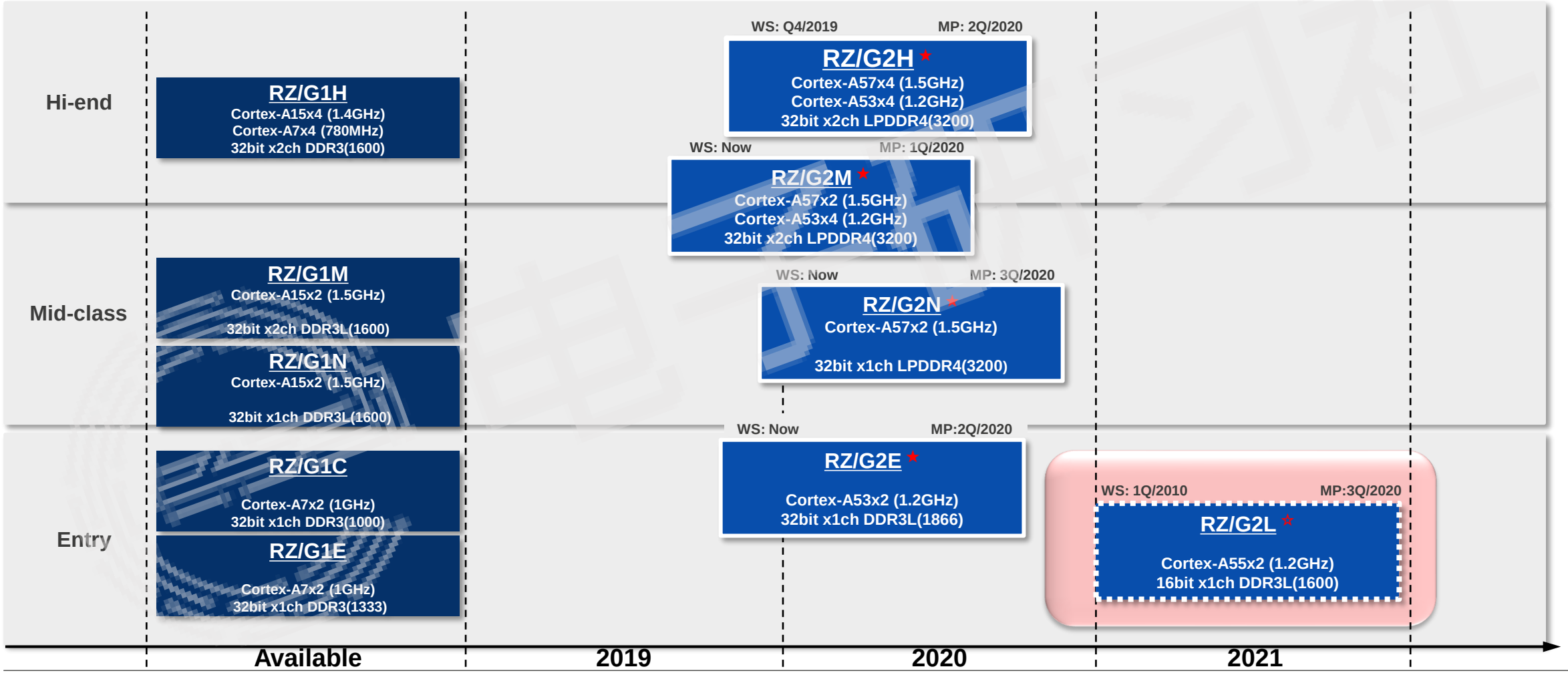
RZ/G Series Roadmap

★ Under development
☆ Under Planning



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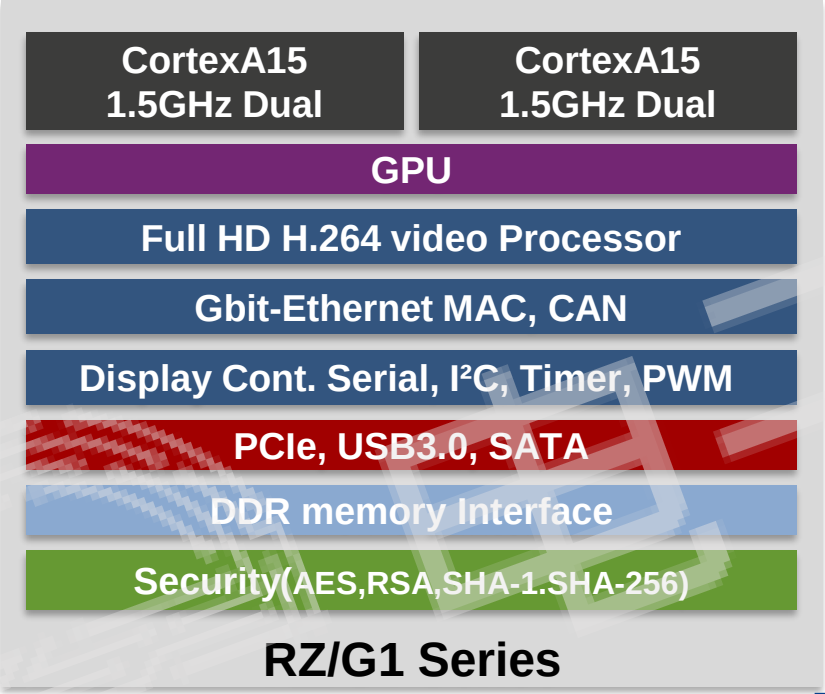
BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G1 Series Features



- Two Powerful ARM® Cortex®-A CPU units with over 1GHz each
- FullHD compatible, equipped with Renesas H.264Codec
- PowerVR optimum for embedded devices in 3DGfx engine
- Built-in high-speed interfaces (USB3.0, SATA, PCI-e, Gbit-Ethernet)
- Security functions for communication, data and program protection

Full HD movies and 3D graphics work without stress
Spare performance that can withstand future function upgrades

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G1 Specifications

	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1C	RZ/G1E
CPU	4x Cortex-A15@1.4GHz 4x Cortex-A7@780MHz (25kDMIPS)	2x Cortex-A15@1.5GHz (10.5kDMIPS)	2x Cortex-A15@1.5GHz (10.5kDMIPS)	2x Cortex-A7@1.0GHz (3.8kDMIPS)	2x Cortex-A7@1.0GHz (3.8kDMIPS)
DRAM I/F	32bit x2ch DDR3-1600	32bit x2ch DDR3L-1600	32bit x1ch DDR3L-1600	32bit x1ch DDR3-1000	32bit x1ch DDR3-1333
Video in	Video In x4ch (Digital)	Video In x3ch (Digital)	Video In x3ch (Digital)	2ch selectable Video In x2(Digital) /CVBS In x1	Video In x2ch (Digital)
Video Codec	Up to Full-HD x 2ch	Up to Full-HD x 1ch	Up to Full-HD x 1ch	Up to Full-HD x 1ch	Up to Full-HD x 1ch
3D GFX	PowerVR G6400@520MHz	PowerVR SGX544MP2@520MHz	PowerVR SGX544MP2@312MHz	PowerVR SGX531@260MHz	PowerVR SGX540@260MHz
Display out	RGB888 x1ch LVDS x2ch	RGB888 x1ch LVDS x1ch	RGB888 x1ch LVDS x1ch	2ch selectable RGB888 x2/ LVDS x1/CVBS out x1	RGB888 x2ch
USB2.0	USB2.0 x2ch	USB2.0 x2ch	USB2.0 x2ch	USB2.0 x2ch	USB2.0 x2ch
Ether	1Gb Ethernet 10-100 Ethernet	1Gb Ethernet or 10-100 Ethernet	1Gb Ethernet or 10-100 Ethernet	1Gb Ethernet or 10-100 Ethernet	1Gb Ethernet 10-100 Ethernet
USB3.0/PCIe/SATA	PCIe /SATA x1ch USB3.0/SATA x1ch	PCIe /SATA x1ch USB3.0/SATA x1ch	PCIe /SATA /USB3.0 x1ch	No	No
Package	831pin 27mm x 27mm 0.8mm ball pitch	831pin 27mm x 27mm 0.8mm ball pitch	831pin 27mm x 27mm 0.8mm ball pitch	501pin 21mm x 21mm 0.8mm ball pitch	501pin 21mm x 21mm 0.8mm ball pitch

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BIG IDEAS FOR EVERY SPACE RENESAS

Function extension points
From RZ/G1 to RZ/G2

	RZ/G1 Group	RZ/G2 Group
CPU	32bit ARMv7-A Cortex-A15 Cortex-A7	64bit ARMv8-A Cortex-A57 Cortex-A53
DRAM I/F	DDR3/DDR3L	DDR3L/LPDDR4 (ECC)
Video	FHD resolutions H.264/AVC	4K resolutions H.265 Decoder H.264/AVC
3D GFX	PowerVR	PowerVR Latest Version
Display out	LVDS, RGB888	HDMI,LVDS,RGB888
Video in	Digital (RGB/YCbCr) Max 4	MIPI-CSI2,Digital (RGB/YCbCr) Max 8
Security	Cryptographic processing engine (AES、DES、Hash function、RSA)	Cryptographic processing engine (AES、DES、Hash function、RSA) TrustZone (Apr.2020)
Other peripheral functions	USB3.0, SATA, PCI-e, Giga Bit Ether	USB3.0, SATA, PCI-e, Giga Bit Ether

Adopted as RZ/G2 board CIP standard

Improve industrial safety and reliability

Supports 4K display

MIPI support for image input

Improved security

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2 SPECIFICATIONS

★ Under development

	RZ/G2H	RZ/G2M	RZ/G2N	RZ/G2E	RZ/G2L★	RZ/G2LC★
	Wide-Range Scalable & Pin compatible Products		(37.6k~14.3k DMIPS)	Economical	Low cost	
CPU	4x Cortex-A57@1.5GHz 4x Cortex-A53@1.2GHz (37.6kDMIPS) Parity/ECC	2x Cortex-A57@1.5GHz 4x Cortex-A53@1.2GHz (25.3kDMIPS) Parity/ECC	2x Cortex-A57@1.5GHz (14.3kDMIPS) Parity/ECC	2x Cortex-A53@1.2GHz (7.5kDMIPS) Parity/ECC	2x Cortex-A53@1GHz (7.5kDMIPS) Parity/ECC	1x Cortex-A53@1GHz (7.5kDMIPS) Parity/ECC
DRAM I/F	32bit x2ch LPDDR4(3200) w/ECC	32bit x2ch LPDDR4(3200) w/ECC	32bit x1ch LPDDR4(3200) w/ECC	32bit x1ch DDR3L(1866) w/ECC	16-bit DDR3L/4 w/ECC	16-bit DDR3L/4 w/ECC
Video in	2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8input image can be captured	2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8input image can be captured	2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8input image can be captured	1xMIPI-CSI2, 1xDigital(RGB/YCbCr) up to 2input image can be captured	Camera Input : MIPI-CSI2 (4lane), Parallel camera interface	Camera Input : MIPI-CSI2 (4lane), Parallel camera interface
Video Codec	Support up to 4k resolutions Decoding : H.265, Encoding and Decoding : H.264	Support up to 4k resolutions Decoding : H.265, Encoding and Decoding : H.264	Support up to 4k resolutions Decoding : H.265, Encoding and Decoding : H.264	Support up to FHD resolutions Decoding : H.265, Encoding and Decoding : H.264	H.264 Hardware Codec (H.264 Encode/Decode, up to FullHD 30fps)	N/A
3D GFX	PowerVR GX6650@600MHz	PowerVR GX6250@600MHz	PowerVR GE7800@600MHz	PowerVR GE8300@600MHz	3D Graphics (Mali-G31)	3D Graphics (Mali-G31)
Display out	1xHDMI, 1xLVDS, 1x Digital RGB	1xHDMI, 1xLVDS, 1x Digital RGB	1xHDMI, 1xLVDS, 1x Digital RGB	2xLVDS or 1xLVDS, 1x Digital RGB	Display output : MIPI-DSI (4lane), Parallel RGB	Display output : MIPI-DSI (4lane)
USB	USB2.0 x 2ch (1H, 1H/F/OTG) USB3.0/2.0 x1ch (DRD)	USB2.0 x 2ch (1H, 1H/F/OTG) USB3.0/2.0 x 1ch (DRD)	USB2.0 x 2ch (1H, 1H/F/OTG) USB3.0/2.0 x 1ch (DRD)	USB2.0 x 1ch (H/F) USB3.0/2.0 x1ch (DRD)	USB2.0 x 1ch (H/F) USB3.0/2.0 x1ch (DRD)	USB2.0 x 1ch (H/F) USB3.0/2.0 x1ch (DRD)
Gbit Ether	1ch	1ch	1ch	1ch	2ch	1ch
PCIe	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	2ch (Rev2.0 1Lane)	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	1ch(Rev2.0 1Lane)	N/A	N/A
SATA	1ch(Pin Shared)	No	1ch（Pin Shared）	No	N/A	N/A
Package	1022pin FCBGA, 29mm x 29mm 0.8mm ball pitch	1022pin FCBGA, 29mm x 29mm 0.8mm ball pitch	1022pin FCBGA, 29mm x 29mm 0.8mm ball pitch	552pin FCBGA, 21mm x 21mm 0.8mm ball pitch	400pin,15mm□(0.5mm pitch) 450pin,21mm□(0.8mm pitch)	**272-pin, 13mm□PBGA (0.5mm pitch)**

Pin Compatible

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2H BLOCK DIAGRAM

Industry grade leading position

CPU system

4x ARM Cortex A57 @1.5GHz
I-L1$: 48KB / D-L1$: 32KB; Parity/ECC
L2$: 2MB; ECC
NEON/VFP; each Core

4x ARM Cortex A53 @1.2GHz
I-L1$: 32KB / D-L1$: 32KB; Parity/ECC
L2$: 512KB; ECC
NEON/VFP; each Core

1x ARM Cortex R7 @800 MHz
I-L1$: 32KB / D-L1$: 32KB;
I-TCM: 32KB / D-TCM:32KB;
VFP (option)

System

- System Controller
- SYSTEM RAM: 384KB
- Thermal Sensor
- JTAG Debug (Coresight)

3D GPU

PowerVR GX6650
2D/3D tile based
600MHz

Video Codec

Up to 4K resolution
(2 channels)

Video IP

- 3x Display Out: 1x Digital out; 1x LVDS; 1x HDMI
- 8x Video In
  2x MIPI-CSI2 (1x4L, 1x2L)
  2x Digital
- 2x VSPB
- 2x VSPI
- 2x FDP

Memory I/F

- 2x 32bit LPDDR4-3200 (ECC) access cache
- Raw NAND (8/16bit, ONFI 1.x, ECC 1-8bits)
- 16bit ExtBus/SRAM
- 1xQSPI (4/8 bit selectable) or 1xHyperflash
- 4x SDIO (SDR104)
- 2x eMMC (5.0, HS400)

Connectivity

- 2x PCIe (Rev2.0, 1 lane)
- SATA (Rev3.2) (shared)
- USB3.0/2.0 (DRD)
- 2xUSB2.0(1H,1H/F/OTG)
- Ethernet AVB (1Gbps)
- 2x CAN2.0B
- 6x UART, 5x H-UART
  4x SPI
  7x I²C; 1x DVFS ctrl

Timer

- 26x 32bit Timer
- 15x 32bit Interval
- WDT
- 7x PWM out

Audio IP

Audio router w/10 ASRC, mixer, 10 I²S (6ch TDM), 90ch Audio DMA

Package

FCBGA: 29x29mm²
1022pins, 0.8mm pitch

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2M BLOCK DIAGRAM

CPU system

2x ARM Cortex A57 @1.5GHz
I-L1$: 48KB / D-L1$: 32KB; Parity/ECC
L2$: 1MB; ECC
NEON/VFP; each Core

4x ARM Cortex A53 @1.2GHz
I-L1$: 32KB / D-L1$: 32KB; Parity/ECC
L2$: 512KB; ECC
NEON/VFP; each Core

1x ARM Cortex R7 @800 MHz
I-L1$: 32KB / D-L1$: 32KB;
I-TCM: 32KB / D-TCM:32KB;
VFP (option)

System

- System Controller
- SYSTEM RAM: 384KB
- Thermal Sensor
- JTAG Debug (Coresight)

3D GPU

PowerVR GX6250
2D/3D tile based
600MHz

Video Codec

Up to 4K resolution
(3 channels)

Video IP

- 3x Display Out: 1x Digital out; 1x LVDS; 1x HDMI
- 8x Video In 2x MIPI-CSI2 (1x4L, 1x2L) 2x Digital
- 1x VSPB
- 1x VSPI
- 1x FDP

Memory I/F

- 2x 32bit LPDDR4-3200 (ECC) access cache
- Raw NAND (8/16bit, ONFI 1.x, ECC 1-8bits)
- 16bit ExtBus/SRAM
- 1xQSPI (4/8 bit selectable) or 1xHyperflash
- 4x SDIO (SDR104)
- 2x eMMC (5.0, HS400)

Connectivity

- 2x PCIe (Rev2.0, 1 lane)
- USB3.0/2.0 (DRD)
- 2xUSB2.0(1H,1H/F/OTG)
- Ethernet AVB (1Gbps)
- 2x CAN2.0B
- 6x UART, 5x H-UART 4x SPI 7x I²C; 1x DVFS ctrl

Timer

- 26x 32bit Timer
- 15x 32bit Interval
- WDT
- 7x PWM out

Audio IP

Audio router w/10 ASRC, mixer, 10 I²S (6ch TDM), 90ch Audio DMA

Package

FCBGA: 29x29mm²
1022pins, 0.8mm pitch

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2N BLOCK DIAGRAM

CPU system

2x ARM Cortex A57 @1.5GHz
I-L1$: 48KB / D-L1$: 32KB; Parity/ECC
L2$: 1MB; ECC
NEON/VFP; each Core

1x ARM Cortex R7 @800 MHz
I-L1$: 32KB / D-L1$: 32KB;
I-TCM: 32KB / D-TCM:32KB;
VFP (option)

System

- System Controller
- SYSTEM RAM: 384KB
- Thermal Sensor
- JTAG Debug (Coresight)

3D GPU

PowerVR GE7800
2D/3D tile based
600MHz

Video Codec

Up to 4K resolution
(1 channels)

Video IP

- 3x Display Out: 1x Digital out; 1x LVDS; 1x HDMI
- 8x Video In
  2x MIPI-CSI2
  (1x4L, 1x2L)
  2x Digital
- 1x VSPB
- 1x VSPI
- 1x FDP

Timer

- 26x 32bit Timer
- 15x 32bit Interval
- WDT
- 7x PWM out

Memory I/F

- 1x 32bit LPDDR4-3200 (ECC) access cache
- Raw NAND (8/16bit, ONFI 1.x, ECC 1-8bits)
- 16bit ExtBus/SRAM
- 1xQSPI (4/8 bit selectable) or 1xHyperflash
- 4x SDIO (SDR104)
- 2x eMMC (5.0, HS400)

Audio IP

Audio router w/10 ASRC, mixer, 10 I²S (6ch TDM), 90ch Audio DMA

Connectivity

- 2x PCIe (Rev2.0, 1 lane)
- SATA (Rev3.2) (shared)
- USB3.0/2.0 (DRD)
- 2xUSB2.0(1H,1H/F/OTG)
- Ethernet AVB (1Gbps)
- 2x CAN2.0B
- 6x UART, 5x H-UART
  4x SPI
  7x I²C; 1x DVFS ctrl

Package

FCBGA: 29x29mm²
1022pins, 0.8mm pitch

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2E BLOCK DIAGRAM

CPU system

2x ARM Cortex A53 @1.2GHz
I-L1$: 32KB / D-L1$: 32KB; Parity/ECC
L2$: 256KB; ECC
NEON/VFP; each Core

1x ARM Cortex R7 @800 MHz
I-L1$: 32KB / D-L1$: 32KB;
I-TCM: 32KB / D-TCM:32KB;
VFP (option)

System

- System Controller
- SYSTEM RAM: 128KB
- Thermal Sensor
- JTAG Debug (Coresight)

3D GPU

PowerVR GE8300
2D/3D tile based
600MHz

Video Codec

Up to FHD resolution

Video IP

- 2x Display Out: (2x LVDS or 1x LVDS + 1x DRGB)
- 2x VideoIn
  1x MIPI-CSI2(1x2L)
  1x Digital
- 1x VSPB
- 1x VSPI
- 1x FDP

Memory I/F

- 1x 32bit DDR3L-1856 (ECC) access cache
- Raw NAND (8bit, ONFI 1.x, ECC 1-8bits)
- 16bit ExtBus/SRAM
- 1xQSPI (4/8 bit selectable) or 1xHyperflash
- 3x SDIO (SDR104)
- 1x eMMC (5.0, HS400)

Connectivity

- 1x PCIe (Rev2.0, 1 lane)
- USB3.0/2.0 (DRD)
- 1xUSB2.0(1H/F)
- Ethernet AVB (1Gbps)
- 2x CAN2.0B
- 6x UART, 5x H-UART
  4x SPI
  8x I²C; 1x DVFS ctrl

Timer

- 26x 32bit Timer
- 15x 32bit Interval
- WDT
- 7x PWM out

Audio IP

Audio router w/8 ASRC, mixer, 10 I²S (3ch TDM), 45chAudio DMA

Package

FCBGA: 21x21mm²
552pins, 0.8mm pitch

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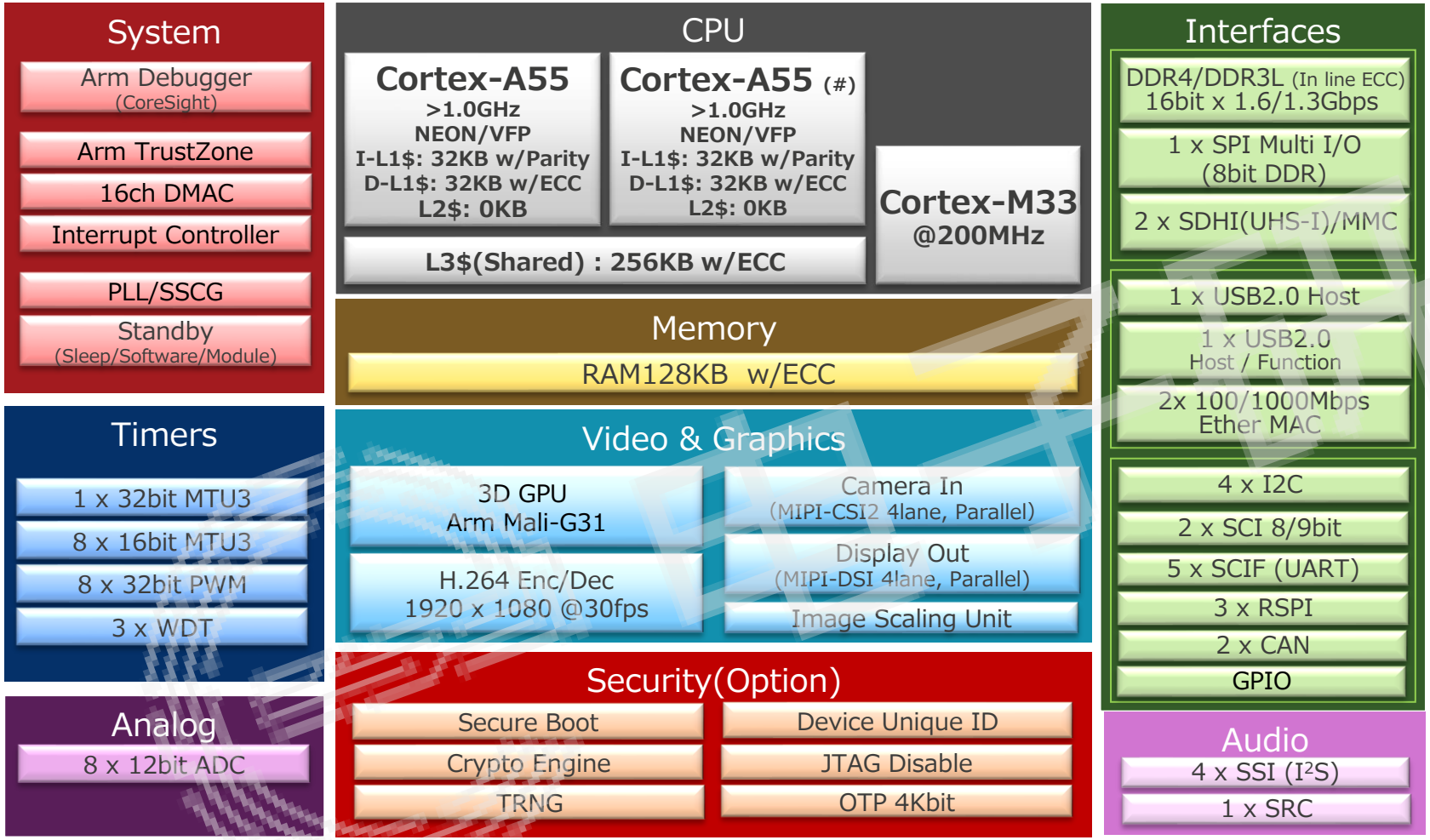
BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2L BLOCK DIAGRAM

2021,Jan sample ready



High performance

- 64bit CPU (Arm Cortex A55 Dual = 1.2GHz)
  (6x ML performance (8bit MAC) than CA53)
- 3D Graphics (Arm Mali-G31)
- H.264 Hardware Codec
  (H.264 Encode/Decode, up to FullHD 30fps)
- Camera Input : MIPI-CSI2 (4lane), Parallel
- Display output : MIPI-DSI (4lane), Parallel
  (up to FullHD 60fps with MIPI-DSI)

High reliability

- CIP Linux (10+year Super Long term support)
- Built-in ECC for Internal & External Memory
- Hardware security (Option)

Package

- 400pin, 15mm□PBGA(0.5mm pitch)
- 450pin, 21mm□PBGA(0.8mm pitch)

Some functions may be reduced in 0.5mm pitch due to package size limitation.

(#) Single Core version is 1CPU.

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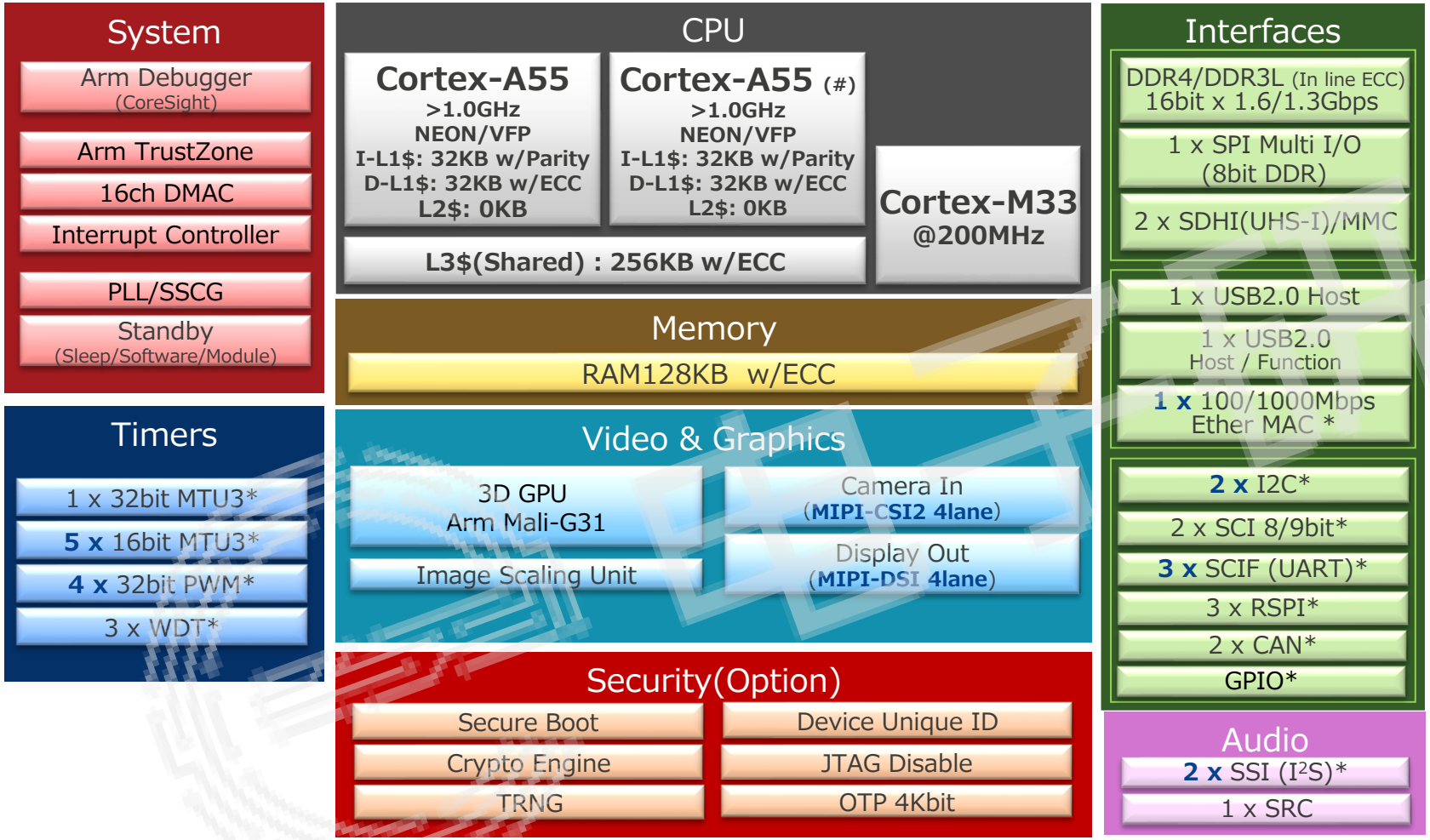
BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2LC BLOCK DIAGRAM

2021,Jan sample ready



*Shared

(#) Single Core version is 1CPU.

High performance

- 64bit CPU (Arm Cortex A55 Dual = 1.2GHz)
  (6x ML performance (8bit MAC) than CA53)
- 3D Graphics (Arm Mali-G31)
- Camera Input : MIPI-CSI2 (4lane)
- Display output : MIPI-DSI (4lane)

High reliability

- CIP Linux (10+year Super Long term support)
- Built-in ECC for Internal & External Memory
- Hardware security (Option)

Package

- 272pin, 13mm□PBGA(0.5mm pitch)

(Blue Character): Channel or Size Number Difference to RZ/G2L

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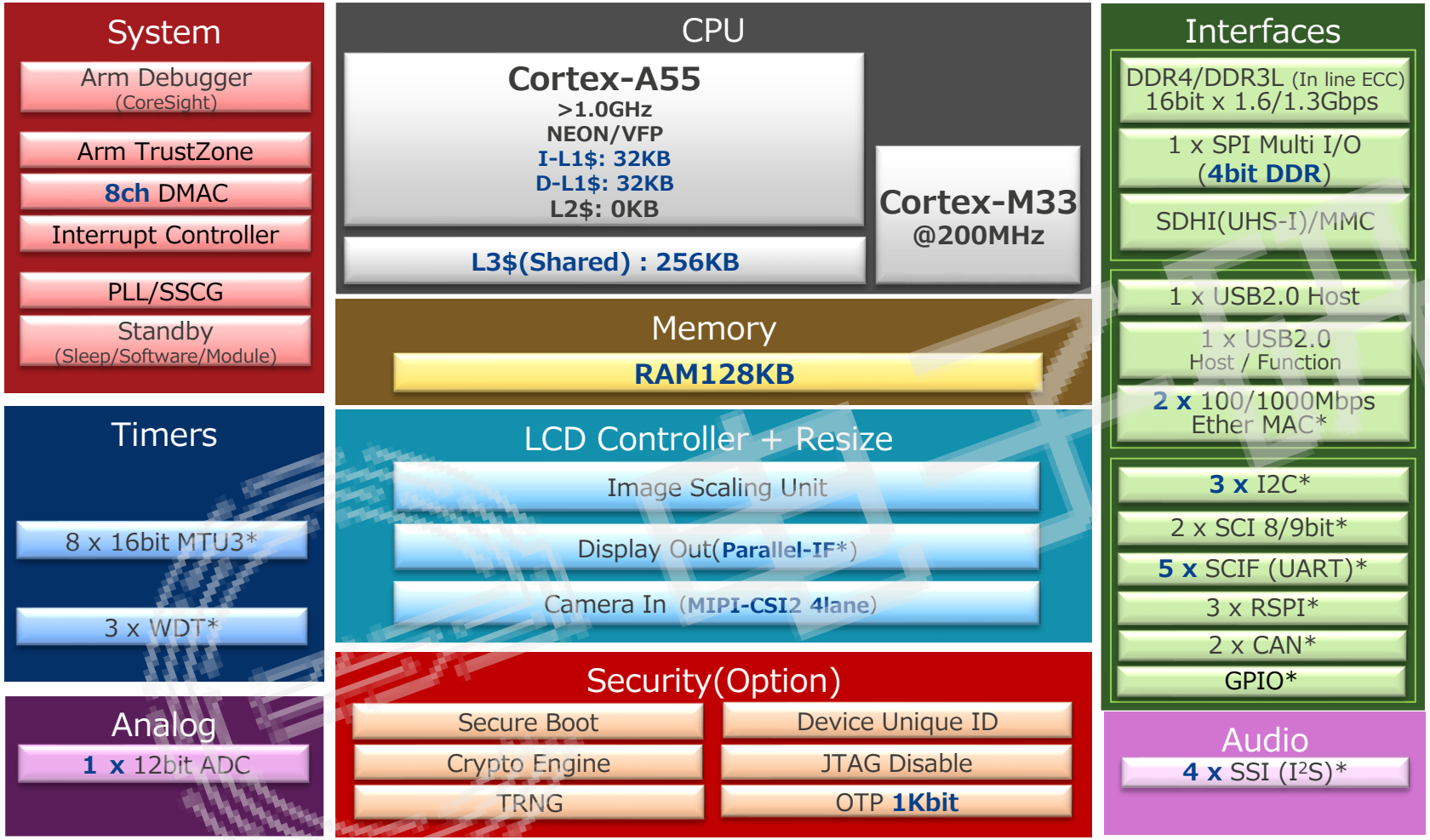
BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2UL BLOCK DIAGRAM

2021,Aug sample ready



*Shared

High performance

- 64bit CPU

  (Arm Cortex A55 Single = 1.2GHz)

- Display output : Parallel
  (up to SVGA 30fps with Parallel)

High reliability

- CIP Linux (10+year Super Long term support)
- Hardware security (Option)

Package

- 298pin, 12mm□PBGA(0.5mm pitch) (T.B.D)

(Blue Character): Channel or Size Number Difference to RZ/G2LC

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BIG IDEAS FOR EVERY SPACE RENESAS

RENESAS RZ/G LINUX SOLUTION

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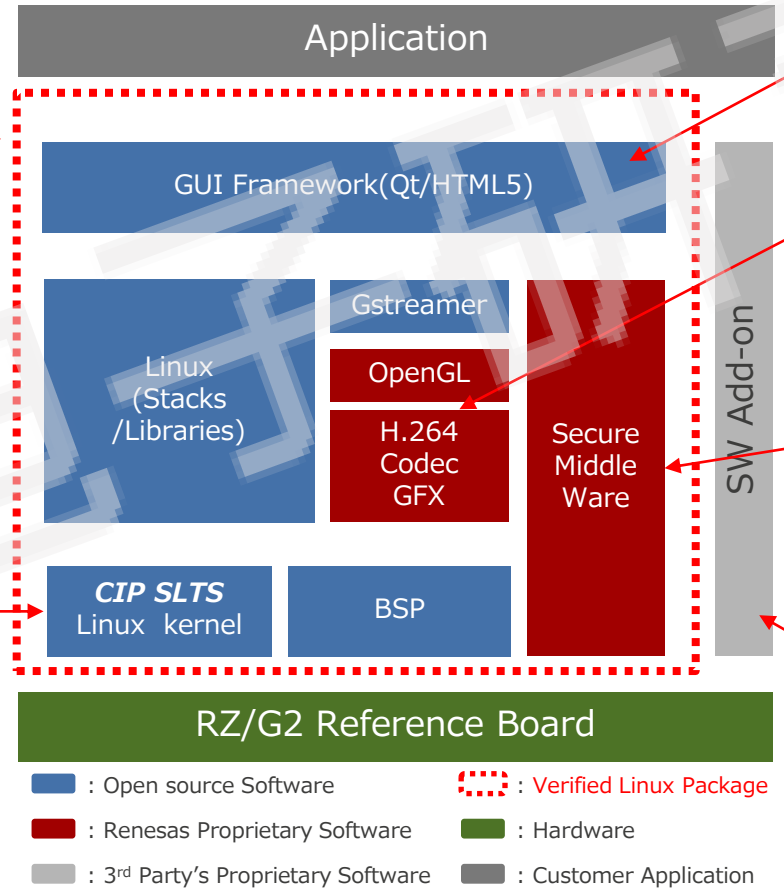
BIG IDEAS FOR EVERY SPACE RENESAS

Verified Linux Package (VLP)

Customers can use verified S/W including middleware necessary for HMI, Application development can start from a stable operating environment

Verified
- Renesas carries out verification
- Software development process management of CMMI level 3
- Provide evidence of verification results



GUI Framework
- Qt application framework
- HTML5 application framework

Multimedia
- H.264 Codec
- H.265 Decoder
- 3D graphics

Secure Middle Ware
- Encrypted kernel boot
- Security communication
- Secure storage

Renesas sample applications

3rd party SW add-on

CIVIL INFRASTRUCTURE PLATFORM

CIP SLTS Kernel
- Civil Infrastructure Platform project
- 10+ years super long term support Reliability/Security/Real-time

(cf. LTSI kernel: 2-3years support)

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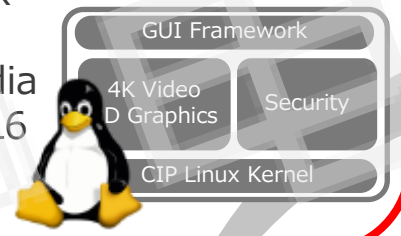
BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G Linux Platform Deliverables

Industry-grade CIP Linux reduces risk and cost of ownership

One package software framework

✓ **Verified Linux Package**
- CIP Linux
- Security
- Multimedia
- Qt/HTML6



RZ/G Processor

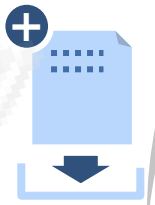
✓ RZ/G1 Series
✓ RZ/G2 Series

Development environment

✓ Linux customization tool
✓ Validation / analysis tool
✓ Smart Configurator

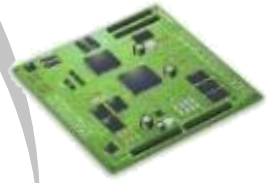
Solution Software Add-on

✓ Unique Partner Middleware



RZ/G Linux Platform

Evaluation Board



✓ Partner Board
- HiHope
- iWave

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BIG IDEAS FOR EVERY SPACE

RZ/G Software Support Policy

- Renesas provides support to the items below for RZ/G Verified Linux Package without additional payment.

	Deliverable	Technical Q&A and issue analysis*1	
		Renesas reference board	Customer board
Customer developed/modified SW	—	No	No*2
Customer added OSS	—	No	No
Validation target OSS in VLP	Source	Yes	No
Renesas developed SW	Source	Yes	Yes
	Binary	Yes	Yes*3

*1 Firstly, customers should investigate which part has a problem: Renesas' deliverables or customer's developed part.
*2 We provide support for the board-dependent changes such as channel numbers and pin configurations.
*3 We provide Q&A support only for the functions which are defined and described in the user's manual.

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2 Key Solutions And Benefits

RZ/G delivers advantages by combining hardware and software.

High Performance

64-bit ARMv8A plus powerful graphics engine and 4K UHD video engine offers higher performance per dollar than competing embedded 64-bit MPUs

- Cortex-A53 CPU and Cortex-A57
- Up to 8 cores
- Power VR 3D Graphics
- H.265 Playback, H.264 Recoding/Playback

High Reliability

Built-in Error Correction Code (ECC) essential for high-reliability mission critical systems. Reduces and or eliminates soft errors

- ECC for internal L1 and L2 cache
- ECC for external DDR memory interfaces
- ECC built into all RZ/G2 products

Super Long Term Support (SLTS)

Civil Infrastructure Platform (CIP) offers 10+ years support for Linux kernel

- Security maintenance for over 10 years
- Real-Time Patches for CIP kernel

RZ/G Verified Linux Package (VLP)

Reduce development cost and time with Renesas verified software for RZ/G MPUs

- VLP tested and maintained by Renesas
- VLP Includes CIP Linux kernel
- Development can start immediately

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G EVALUATION KIT INFO (H/W)

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RZ/G Board Information

■ RZ / G evaluation boards are provided by our partners

VLP reference board

Supplier	Device	Board Name
iWave Japan	RZ/G1H	RZ/G1H Q7 Dev.
	RZ/G1M	RZ/G1M Q7 Dev.
	RZ/G1N	RZ/G1N Q7 Dev.
	RZ/G1C	RZ/G1C Dev.
	RZ/G1E	RZ/G1E SODIMM Dev.
	RZ/G2E	EK874
Hoperun	RZ/G2M	HiHOPE-RZG2M
	RZ/G2N	HiHOPE-RZG2N

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G1 Reference Board

- These boards are reference boards for the RZ / G Linux platform

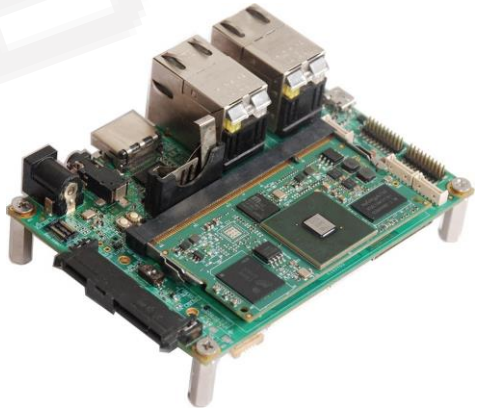
RZ/G1C Single board computer

85.6mm x 56.5mm

RZ/G1E SODIMM

67.6mm x 37mm
SODIMM Size Compact SOM

RZ/G1E SODIMM Development Kit



RZ/G1H Q7 SOM

RZ/G1M Q7 SOM

RZ/G1N Q7 SOM

70mm x 70mm Q7 SOM

RZ/G1x Q7 Development Kit

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2 Reference Board

HiHOPE-RZG2M

(Made by Hoperun)

- Processor ：RZ/G2M
- Main Memory： 4GB LPDDR4
- QSPI NOR FLASH 64MByte
- I2C EEPROM 512Byte
- External Storage: micro SD x1
- Connectivity：
  USB2.0x 2ch, USB3.0x1ch, GbEx1
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi+BT
- PMIC intersil
- Dimension: 54 mm x 85 mm

EK874

(Made by Silicon Linux)

- Processor ：RZ/G2E
- Main Memory： 2GB DDR3L
- QSPI NOR FLASH 64MByte
- I2C EEPROM 512Byte
- External Storage: micro SD x1
- Connectivity：
  USB2.0x 2ch, USB3.0x1ch, GbEx1
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi+BT
- PMIC intersil
- Dimension: 54 mm x 85 mm

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/G2 BOARD AVAILABILITY(2)

- **If customers needs many boards, they can purchase directly from the contacts shown below**
- **The evaluation boards will be available on the website from December**

RZ/G2M evaluation board : HiHOPE-RZG2M

US and Europe
Shenzhen Xuanhuo Tribe Technology Co.Ltd
Contact: Liu Xinghua （Leo Liu）
E-mail: leo.liu@limenamics.com
Phone:+86 135-6076-4801

Asia Pacific
Jiangsu HopeRun Software Co.,Ltd.
Contact: Wang XiangYu
Email: wang_xiangyu1@hoperun.com
Phone: +86 186-5293-0035

RZ/G2E evaluation board : EK874

All regions
iWave Japan Co., Ltd.
Contact: Takefumi Sunagawa
E-mail: info@iwavejapan.co.jp
Phone:+81 45-227-7626

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RZ/G2 BOARD SUPPORT

- **Schematic, BOM, and design data of RZ/G2 evaluation board available on Renesas Sales Gateway since August**

Upload schedule to Renesas Sales Gateway
RZ/G2E : End of November 2019
RZ/G2M : End of November 2019
＊If needed earlier, please contact RZ/G Biz. Dev. member

Upload

Schematics
BOM List
Design Data
(gerber-data)

Download
and
Provide to Customers

Renesas Sales Gateway
https://extranet.renesas.com/

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RENESAS MARKET PLACE (S/W)

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Your development schedule can be accelerated

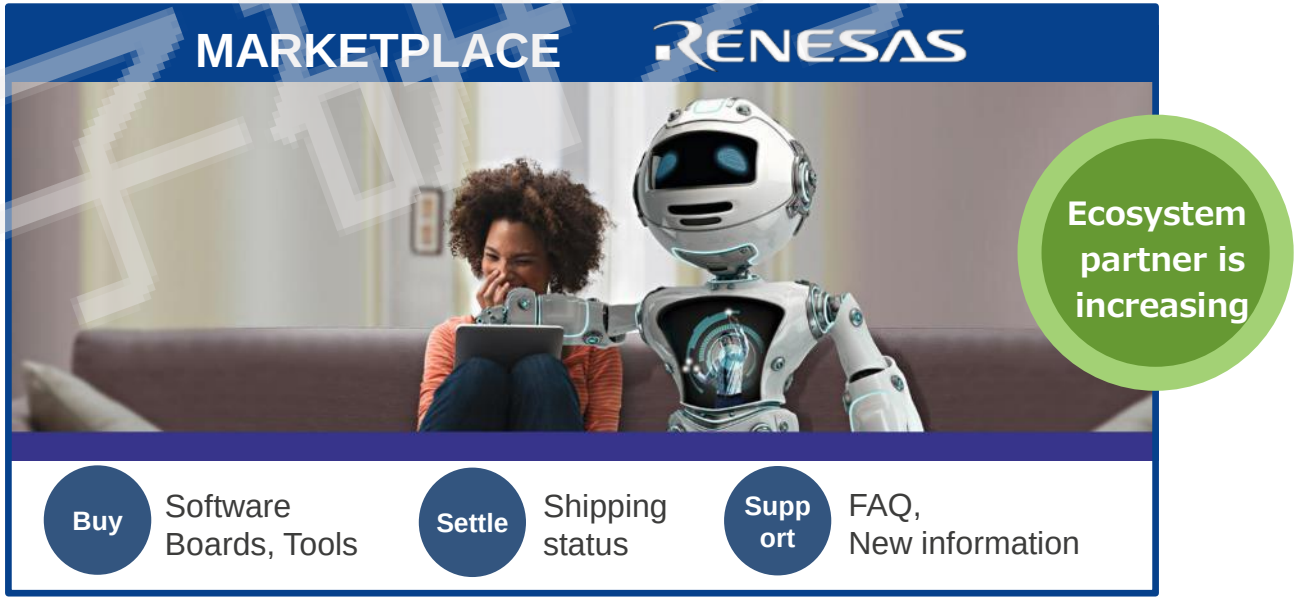
"All the information you want is here"

First in the semiconductor industry

Connect the ecosystem with customer

https://mp.renesas.com/en-us/rzg/index.html

Let's access !!



- Renesas partner 's software products are sold
- Can be one stop shopping which you want

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Recommended development flow and reference items

電子研究社

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BIG IDEAS FOR EVERY SPACE RENESAS

Recommended development flow (for RZ/G2)

Step1

- Perform initial functional evaluation with our evaluation board and BSP(VLP)

Step2

- Refer to our evaluation board, and design a custom board

Step3

- Refer to our BSP, and port the BSP to custom board

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Step1: Necessary items and how to get them

Category	Items	Contents	Offer from	Remark
HW	Board	RZ/G2M,N,H Eva Board (HiHOPE-RZG2M,N,H) RZ/G2E Eva Board (EK847)	RZ/G2M, E: Purchase @Web (Jan, 2020) RZ/G2N: Purchase @Web (Apr, 2020) RZ/G2H: Purchase @Web (Jun, 2020)	Please contact the RZ/G Biz. Dev. Member till available @Web
HW	Doc	Eva Board User's Guide	RZ/G2M,N: Sales Gateway (Dec, 2019) RZ/G2N: Sales Gateway (Mar, 2020) RZ/G2H: Sales Gateway (May, 2020)	Before Dec, Contact to REL
SW	BSP	Verified Linux Package	Market Place site	Now: G2M,G2E Oct: G2N, Jan: G2H
HW	Doc	User's Manual/Hardware: Rev0.80 User's Manual/Hardware: Rev1.00	Rev0.80: from REL Rev1.00: from WEB site (Mar, 2020)	G2H is not available till Rev1.00 Please contact to REL before Mar
HW	Doc	Reference power consumption guide(typ.) for use case	RZ/G2M,N: Sales Gateway (Now) RZ/G2E: Sales Gateway (Nov, 2019) RZ/G2H: Sales Gateway (Mar, 2020)	Before Sales Gateway, Send from REL
SW	Doc	RZ/G Verified Linux Package Start-Up Guide	Market Place site (A revision for RZ/G2 is available by Dec,2019)	Current document is for RZ/G1, but most part of it is useful for RZ/G2 development.
SW	Doc	RZ/G2 Yocto recipe Start-Up Guide	Market Place site (now)	
SW	Doc	RZ/G2 Group BSP Manual Set	Market Place site (now)	
SW	Tool	RZ/G Linux Platform Development Environment	Market Place site	

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Step2: Necessary items and how to get them

Category	Items	Contents	Offer from	Remark
HW	Reference Data	Eva Board Design data (Schematic & Layout data)	RZ/G2M, E: @Board Vendor Site (Nov, 2019) RZ/G2N: @Board Vendor Site (Jan, 2020) RZ/G2H: @Board Vendor Site (Apr, 2020)	Data will be also available @ Sales Gateway. Note that G2N,H board design can refer to G2M due to pin compatibility.
HW	Doc/ Guide	Pin function table	Rev0.81: from REL Rev1.00: Sales Gateway (Feb, 2020)	G2H is not available till Rev1.00 Please contact to REL before Feb
HW	Doc/ Guide	Thermal Management Guideline	RZ/G2M, E: Sales Gateway (Now) RZ/G2N: Sales Gateway (Dec, 2020) RZ/G2H: Sales Gateway (Mar, 2020)	Before Sales Gateway, Send from REL
HW	Doc/ Guide	Design and Verification Guideline for LPDDR4 / DDR3L	RZ/G2M, E: Sales Gateway (Now) RZ/G2N: Sales Gateway (Dec, 2020) RZ/G2H: Sales Gateway (Mar, 2020)	Before Sales Gateway, Send from REL
HW	Model/ Guide	IBIS mode	RZ/G2M, E: Sales Gateway(Nov, 2019) RZ/G2N: Sales Gateway (Dec, 2019) RZ/G2H: Sales Gateway (Feb, 2020)	Before Sales Gateway, Send from REL
HW	Doc/ Guide	Design Guidelines for High Speed Serial Interface	RZ/G2N, M, E: Sales Gateway(Now) RZ/G2H: Sales Gateway (Mar, 2020)	Before Sales Gateway, Send from REL
HW	Tools	Smart Configurator	Renesas site(Now)	https://www.renesas.com/eu/en/products/software-tools/tools/solution-toolkit/smart-configurator.html

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Step3: Necessary items and how to get them

Category	Items	Contents	Offer from	Remark
SW	Doc/ Guide	RZ/G Series Linux BSP Porting Guide	Market Place site (Updated revision for RZ/G2 is available by Dec,2019)	Current revision is for RZ/G1. A draft revision for RZ/G2 can be delivered individually.

Web site information

[Market Place site]
https://mp.renesas.com/en-eu/rzg/marketplace/linux_package/rzg2-vlp-eva.html
https://mp.renesas.com/en-eu/rzg/marketplace/document/RZGD000071.html
https://mp.renesas.com/en-eu/rzg/marketplace/document/RZGD000070.html

[Sales Gateway site]
https://extranet.renesas.com/en/products/microcontrollers-microprocessors/rz/rzg.html#salescollaterals

[RZ/G Linux Platform site]
https://www.renesas.com/eu/en/products/rzg-linux-platform/get-started.html#development-b

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RZ/A SERIES

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BIG IDEAS FOR EVERY SPACE RENESAS

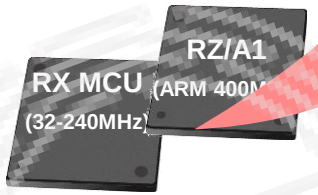
Device Roadmap

- e-AI Class-3 devices have powerful HW AI Engine(DRP-AI).
- Enhance cognitive solution furthermore with these strong AI accelerator devices.

CY2017 | CY2019 | CY2019 | CY2020 | CY2021 | CY2022

[Device roadmap]

e-AI Class-1



x10

WS : Done
MP : 2019/3Q

e-AI Class-2

x10

e-AI Class-3

x10

e-AI Class-4

[Solution roadmap]

2D Barcode Scanner
18/3Q Release

IRIS Scanner
19/1Q Release

Face Recognition
& Authentication

California
123-456

Automatic License
Plate Recognition

To be continued
(Colored area is under planning)

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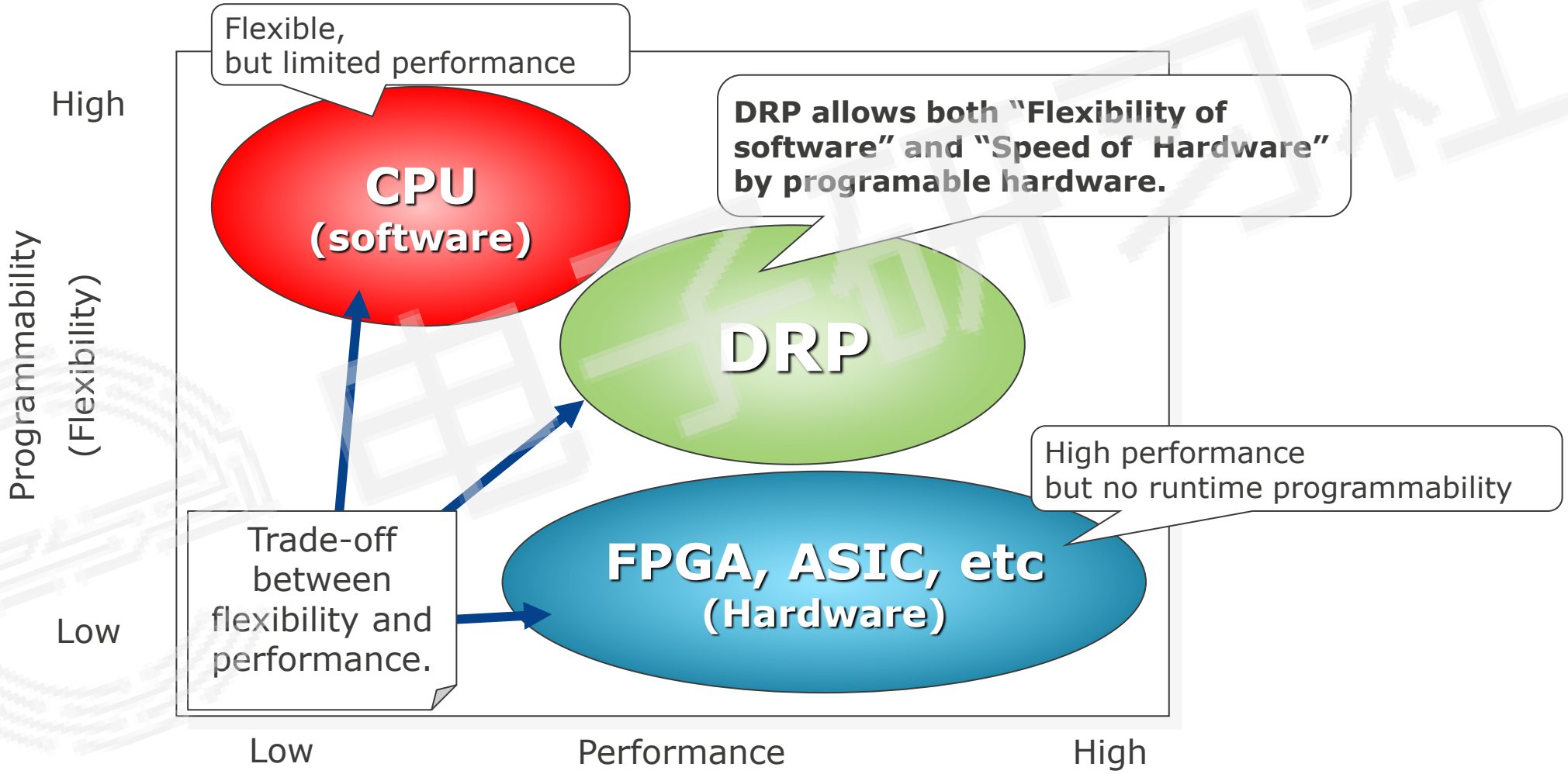
BIG IDEAS FOR EVERY SPACE RENESAS

DRP (Dynamically Reconfigurable Processor)

DRP is the programable hardware which has both "Flexibility of software" and "Speed(Performance) of hardware"



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BIG IDEAS FOR EVERY SPACE
RENESAS

Line up of RZ/A series

*1 There are freq. limitation
*2 Can be used simultaneously
*3 Option
*4 For industry, consumer

Item	RZ/A1H, RZ/A1M	RZ/A1LU	RZ/A1L	RZ/A1LC	RZ/A2M
CPU/Frequency	Cortex-A9/400MHz				Cortex-A9/528MHz
On-chip RAM	5MB／10MB	3MB		2MB	4MB
Flash ROM	NOR, Serial(DDR*1), NAND	NOR, Serial(DDR)	NOR, Serial(SDR)		NOR, Serial(DDR), NAND, HyperFlash
RAM I/F	SDRAM				SDRAM, HyperRAM
Graphics Acc.	2D(OpenVG)	No			2D
LCD out	VDC5(2ch)	VDC5(1ch)			VDC6(1ch)
Camera I/F	Digital(Parallel) Analog(composite)	Digital (Parallel)			Digital (Parallel/serial:MIPI)
JPEG Codec Unit	Yes		No		Yes
Ethernet	10/100base Ether, x 1, EthenetAVB x1		10/100base Ether x 1		10/100base Ether x2*2, (IEEE1588)
Connectivity	USB2.0 x 2 (FS/HS) SD x 2				USB2.0 x 2(FS/HS/OTG) SD x 2(UHS-I)
Security	Secure Boot *3				Secure Boot *3 Crypto engine *3
Package	256QFP, 324BGA 256BGA*4	176QFP, 208QFP, 176BGA*4	176QFP, 208QFP, 176BGA*4	176BGA*4	324BGA*4, 272BGA*4, 256BGA*4, 176BGA*4
Status	MP	MP	MP	MP	Under developing

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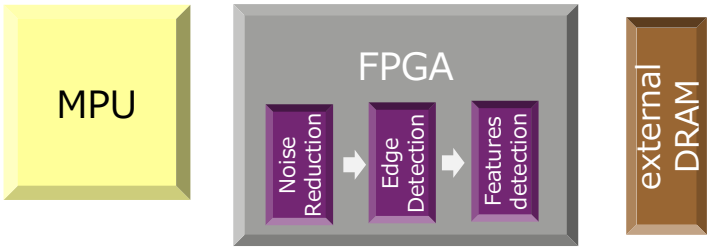
FLEXIBILITY BY DYNAMIC LOADING

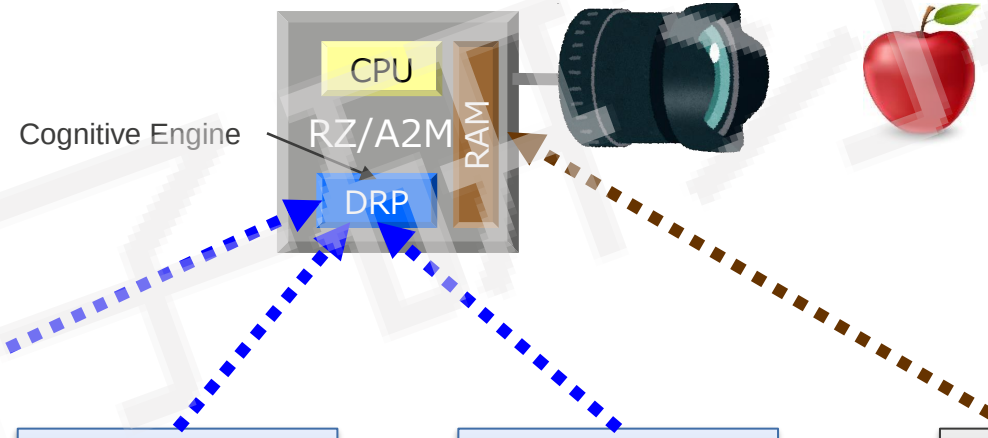
By taking advantage of the short switching time less than 1 ms, the circuit is dynamically replaced every processing step required for object recognition.

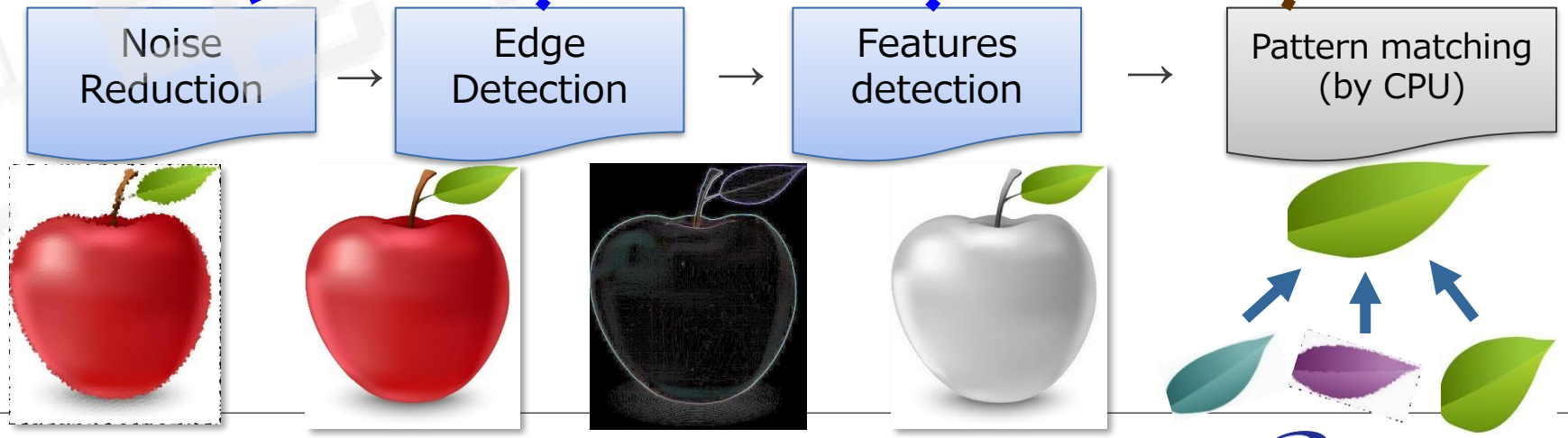
→ Provide flexibility and efficiency that can not be provided by fixed HW of FPGA.

Conventional example when image processing is implemented by FPGA
(It is necessary to implement all required processing circuits)



Example of image processing by DRP





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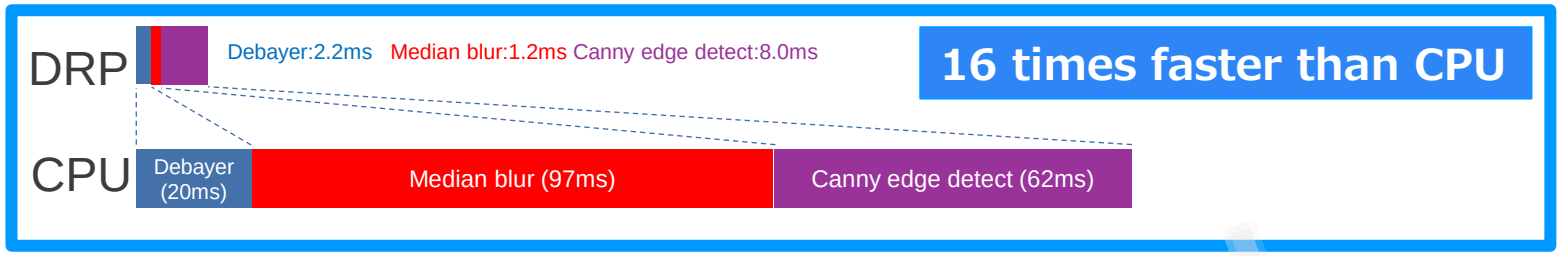
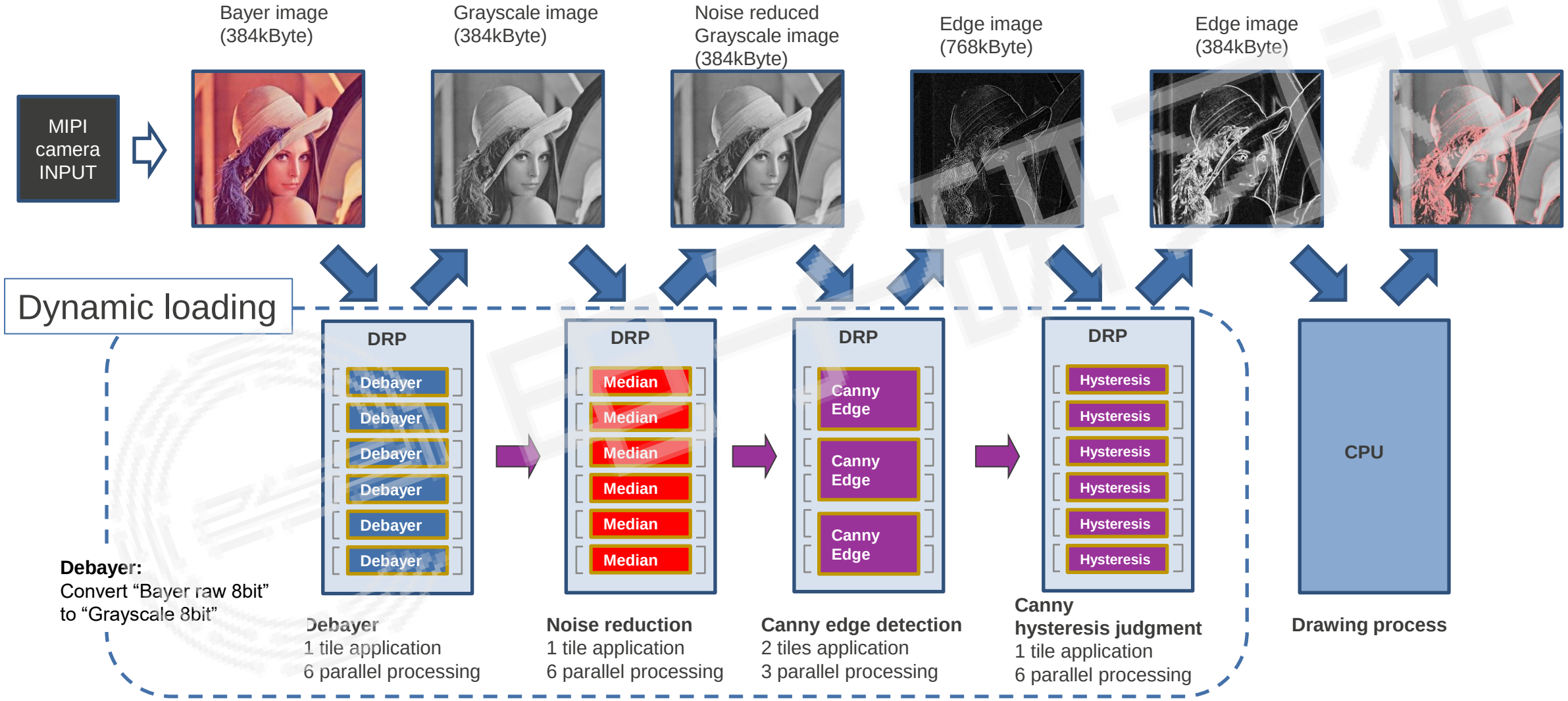
EXAMPLE: CANNY EDGE DETECTION





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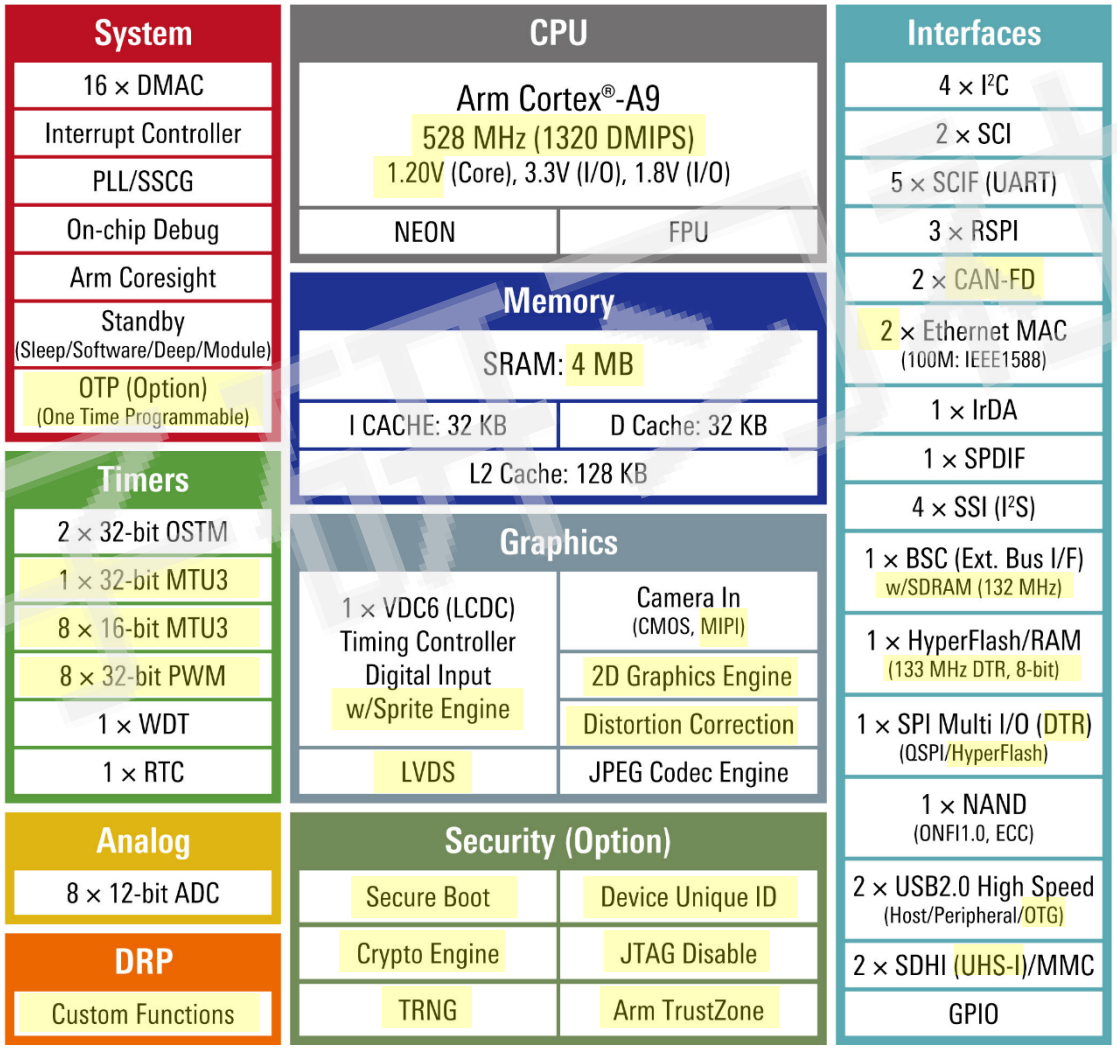
RZ/A2M

FIRST RZ WITH DRP

- **e-AI Class-2**
  - DRP Multipurpose Accelerator
- **Large 4MB SRAM**
  - High-speed access & Low BOM Cost
- **High performance**
  - Cortex-A9 528MHz with NEON DSP
  - 2D Graphics accelerator & Sprite Engine
  - Lens-distortion correction
  - JPEG Hardware codec
- **Security**
  - Arm TrustZone
  - Trusted Secure IP (TSIP)
  - Hardware crypto acceleration
  - Key management and storage
  - Access management
- **Packages**
  - 324pin BGA: 19mm/0.8mm pitch
  - 272pin BGA : 17mm/0.8mm pitch
  - 256pin BGA: 11mm/0.5mm pitch
  - 225pin BGA: 8mm/0.5mm pitch (Under planning)
  - 176pin BGA: 13mm/0.8mm pitch



= Different from RZ/A1

Winner!
Electronic PRODUCTS
PRODUCT OF THE YEAR
2018 AWARD WINNER

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DRP LIBRARY PERFORMANCE

Image size : 640x480 VGA
Image color : Grayscale 8BPP
CPU : RZ/A2M Cortex®-A9@528MHz
RAM : RZ/A2M internal RAM

Category	Function	Tiles	Processing performance [ms]			Note
			DRP	CPU	vs CPU	
Image processing	Simple ISP(Bayer to Color)	6	10.87	-	-	
		3	22.22	-	-	
	Simple ISP(Bayer to Grayscale)	6	6.25	-	-	
		3	13.70	-	-	
Color conversion	Bayer to Grayscale	1	0.85	15.3	x 18.0	6 Parallel Processing
	RGB to Grayscale	1	0.61	5.9	x 9.7	6 Parallel Processing
	Binarization(Fixed)	1	0.18	2.3	x 12.8	6 Parallel Processing
	Binarization(Adaptive)	3	1.69	10.1	x 6.0	
Image filtering	Median filter	1	0.85	76.1	x 89.5	6 Parallel Processing
	Gaussian filter	1	0.85	14.4	x 16.9	6 Parallel Processing
	Unsharp masking	2	1.67	34.1	x 20.4	3 Parallel Processing
	Gamma correction	1	0.23	3.8	x 16.5	6 Parallel Processing
Geometric transformation	Cropping	1	0.06	0.2	x 3.3	6 Parallel Processing
	Resize Bilinear Fixed	4	2.24	2.7	x 1.2	
	Resize Bilinear	6	1.29	3.1	x 2.4	
	Resize Nearest	6	0.33	0.6	x 1.8	

Note: Product is still in development, and performance data is subject to change

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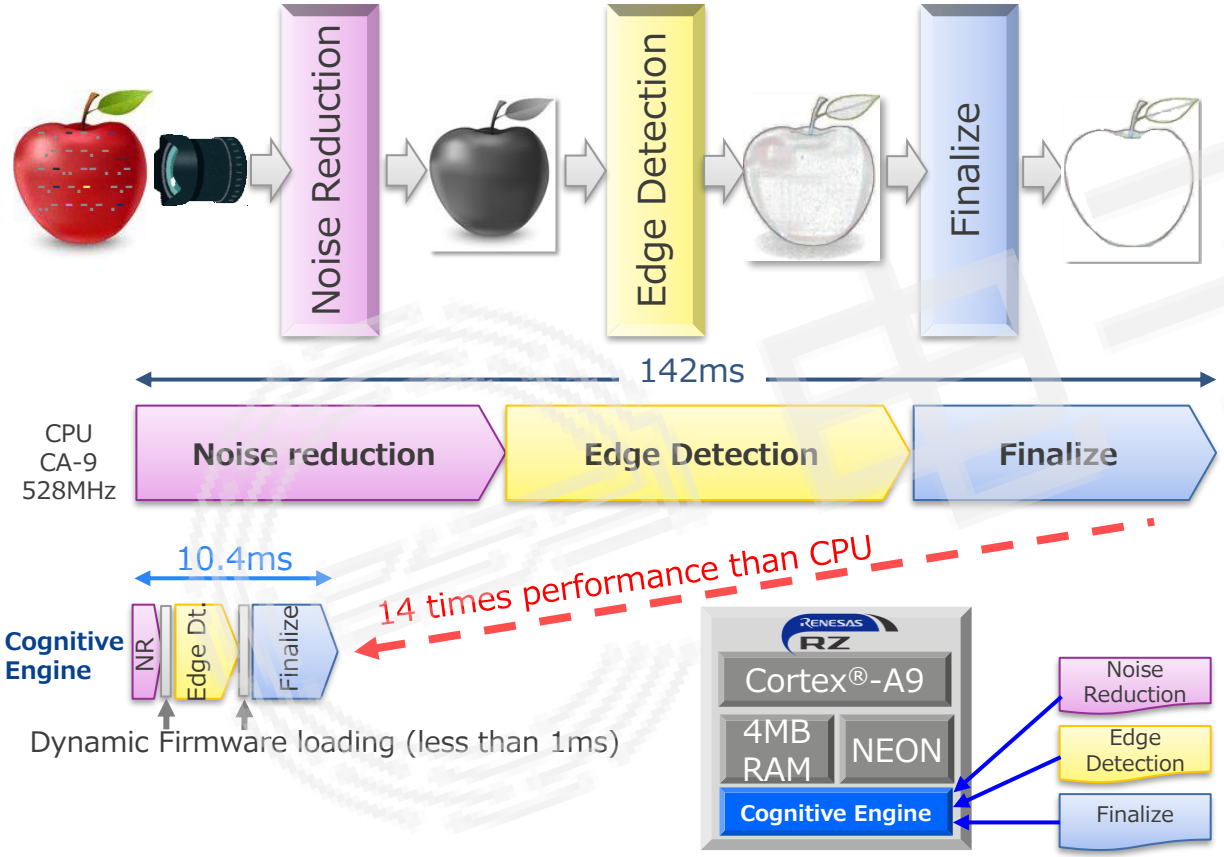
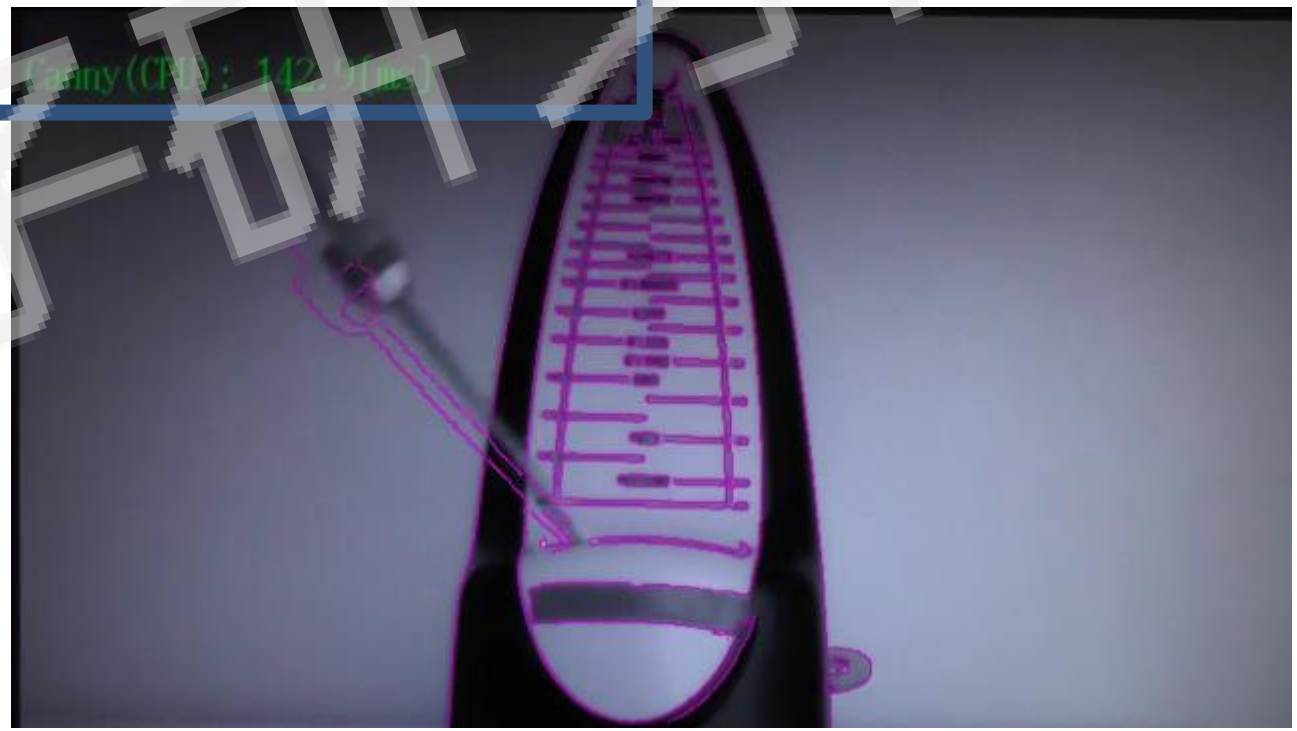
BIG IDEAS FOR EVERY SPACE RENESAS

Benefit (1) DYNAMIC LOADING (DEMO MOVIE)

DRP can execute 'Canny' edge detection ten times faster than CPU.
The application contains three independent process.
DRP can switch and execute these process in 10ms using 'Dynamic Loading' capability.



processing time for one frame



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Projector Only

Benefit (2) ~Energy Efficiency~

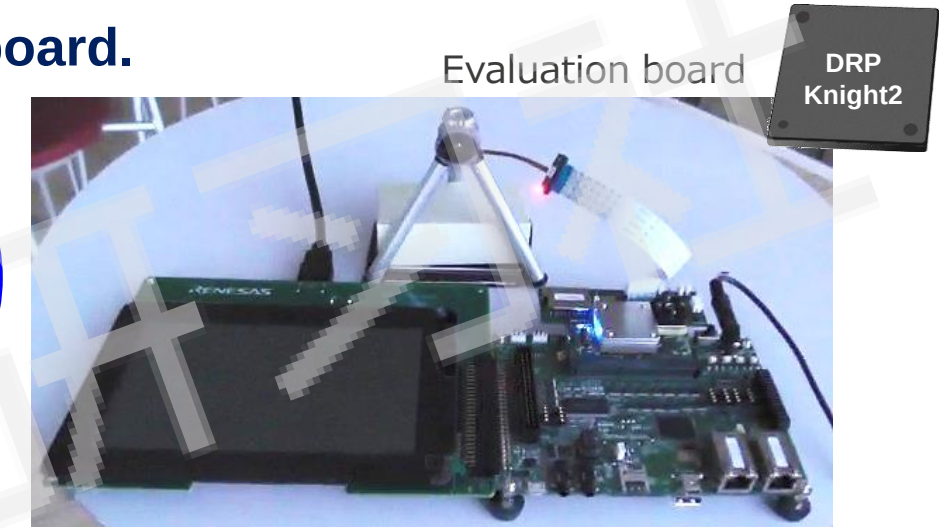
■ DRP achieve less than 1/20 energy of CPU for image processing

- **We measure power consumption using the RZ/A2M board.**

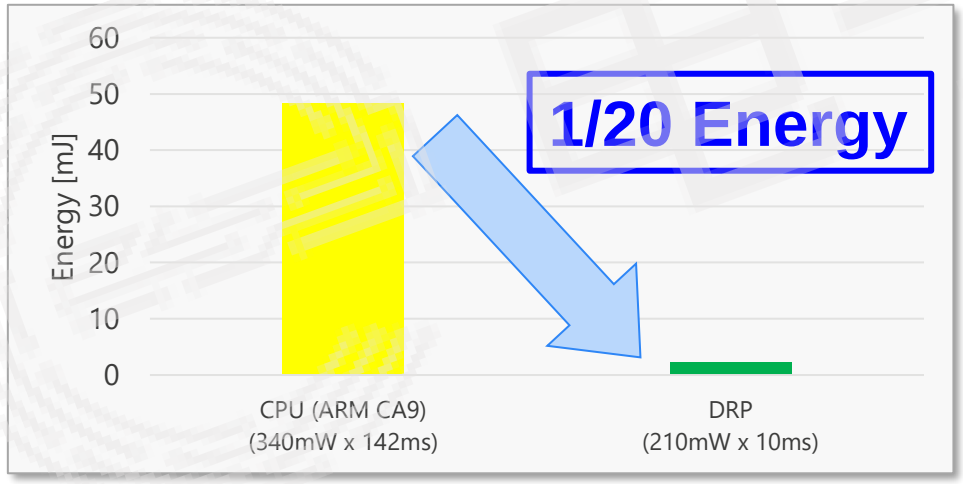
		Operation Frequency	Power Consumption	Execution time	Energy
CPU	Cortex-A9	528MHz	340mW	142 ms (average)	**48 mJ**
DRP	(Class-2) 288 PEs x 64 states	0-66MHz (variable)	210mW	10.4ms (fixed)	**2.2 mJ**

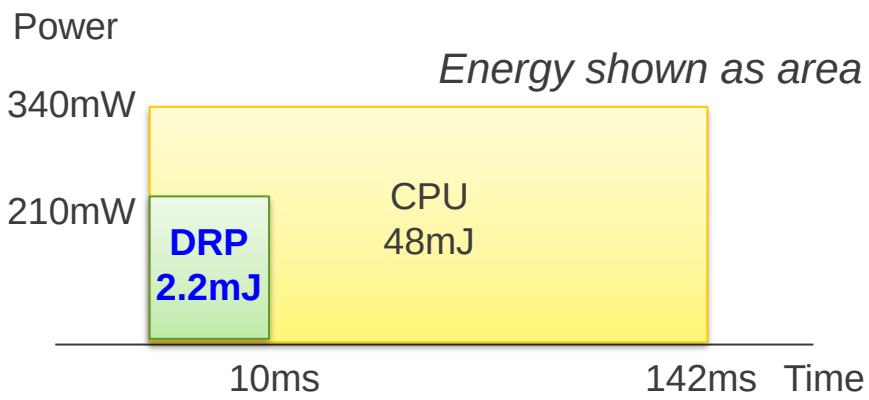
(Condition : typical; room temp. Vdd=1.2V)

Evaluation board



RZ/A2M board





Energy Efficiency Comparison (in Canny Edge Detection per one frame)

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RZ/V SERIES

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BIG IDEAS FOR EVERY SPACE RENESAS

RZ/V2M LSI SPEC

Under development

System
- 16 x DMAC
- Interrupt Controller
- PLL/SSCG
- JTAG Debug（Coresight）

Sensor I/F
- MIPI CSI

Analog
- 12 x ADC(12bit)
- 8 x ADC(12bit)

Peripherals
- 3 x WDT
- 32 x TMR
- 4 x IIC
- 6 x CSI
- 2 x UART
- 16 x PWM
- Audio(I2S)

CPU

ARM Cortex™-A53 1GHz		ARM Cortex™-A53 1GHz	
NEON	FPU	NEON	FPU
L1 I$:32KB	L1 D$:32KB	L1 I$:32KB	L1 D$:32KB

L2$: 128KB

Video Subsystem
- H.264/265 Multi Codec
- 2D Graphics

DRP
- **DRP** (STP3B)
- **DRP+AI-MAC** (STP3B-AI)

Interfaces
- 1 x SDIO
- 1 x PCI-e Gen2 (2Lane)
- 1 x Gbit Ethernet MAC
- 1 x USB3.1 SuperSpeed (Host/Peripheral)
- 1 x MIPI DSI/Parallel (4Lane)
- GPIO

Memory I/F
- LPDDR4-3200 32bit x 1ch
- 1 x eMMC
- 1 x NAND
- 1 x SDXC

Security
- Security IP

Schedule
- ■Device : ✓ WS : Apr ’20. ✓ MP : Dec ’20 ✓ Manual: Sep ’19(α)
- ■Development Environment : ✓Linux BSP: Apr ‘20(α) Sep ’20(β)
  ✓e-AI Translator : Jun ’19(α) Sep’19(β)

Power supply : 0.8V(Core), 3.3V/1.8V/1.2V/1.1V(I/O)
Package: 841pin FCBGA □ 15mm/0.5mm pitch

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Projector Only

Demonstration (object recognition by TinyYOLO neural network)

Intel Myriad 2 (SHAVE x12, 600MHz, TinyYOLO/FP16)

Class-3 DRP-AI Test-chip (FP16 MAC x1024, 400MHz, TinyYOLO/FP16)

Judgement threshold | AI processing time of DRP-AI | Post processing time of CPU | frame rate

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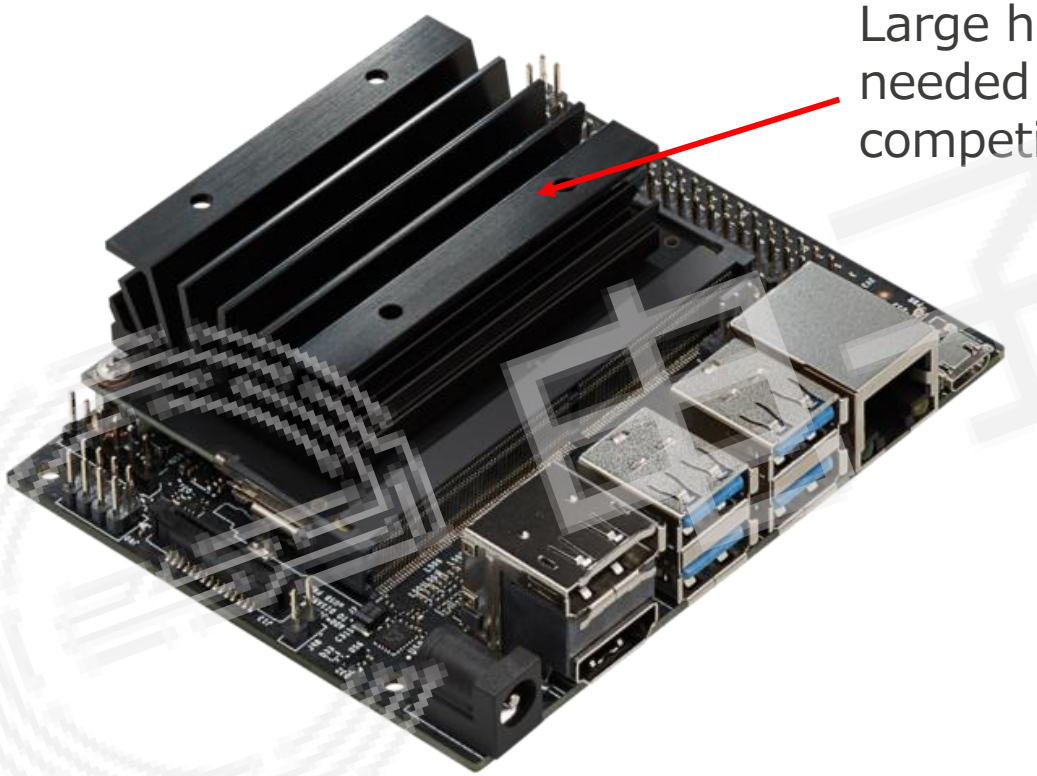
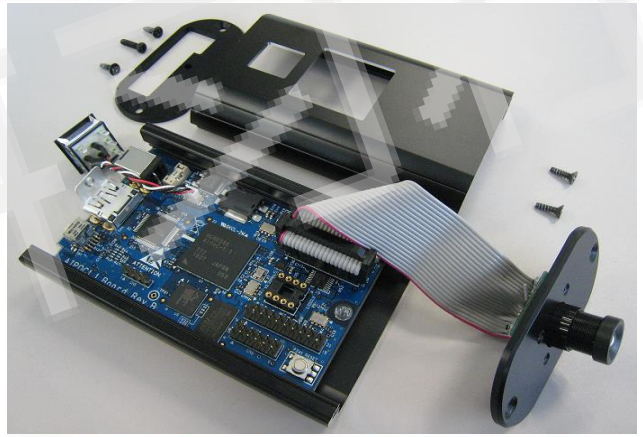
Heat Dissipation Comparison (DRP-AI vs. GPU)

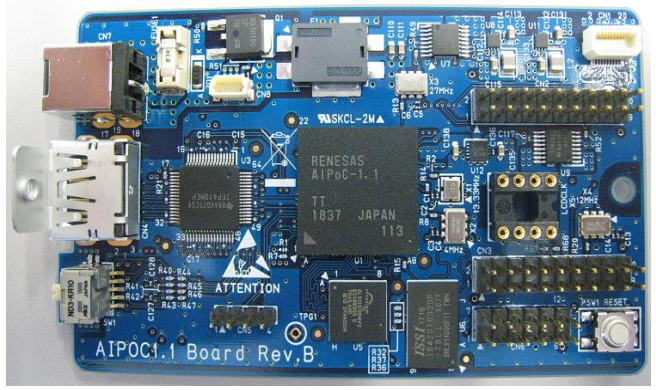
GPU requires big heatsink for heat dissipation to secure normal operation
But, DRP-AI (built-in RZ/V2M) does NOT require any heatsink for heat dissipation
→ BoM Cost and Board Space can be significantly reduced



Large heatsink is needed for competitor's board.

Jetson Nano Developer Kit (80x100mm)





RZ/V2M Demo Board

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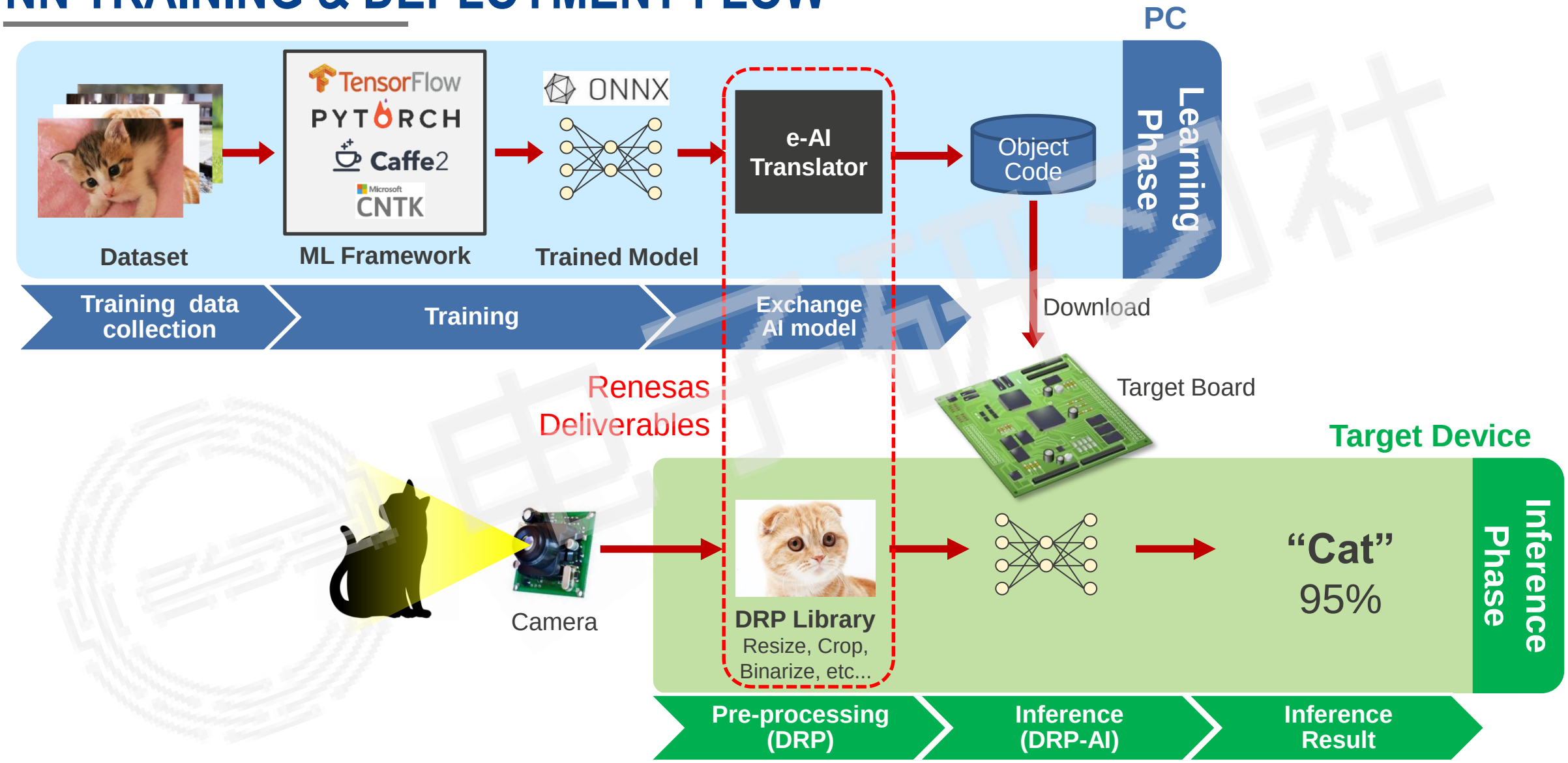
NN TRAINING & DEPLOYMENT FLOW



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