Meeting (EMI) requirements with CoolMOS™

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Learning objectives

After attending the training, you will be able to

- Replace standard MOSFET with CoolMOS™ and successfully meet EMI
- Replace previous CoolMOS™ Generations and competitor Super Junction MOSFETs with CoolMOS™ P7 / CE MOSFETs and successfully meet EMI
- Make new designs with CoolMOS™ P7 / CE based power supplies and successfully meet EMI

Agenda

1 Introduction

2 Methods to improve CoolMOS™ EMI behaviour

- External Rg
- External Cgd
- External Cds
- Ferrite beads
- Transformers

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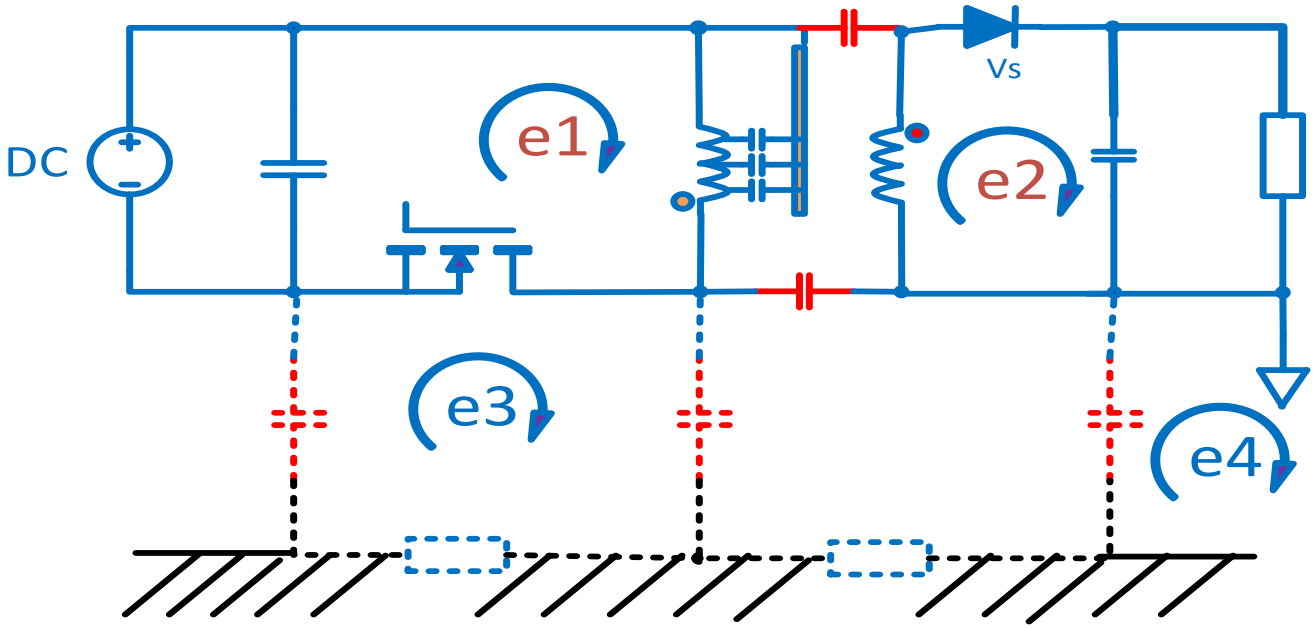
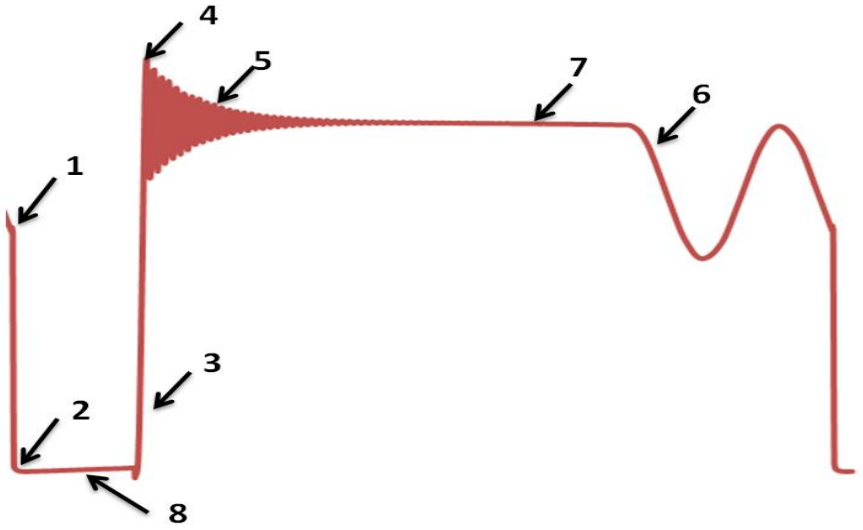
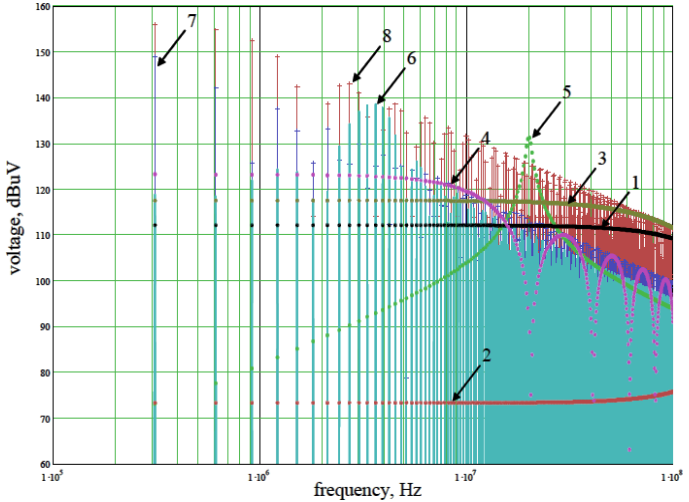
Noise source



Waveform products frequency spectrum





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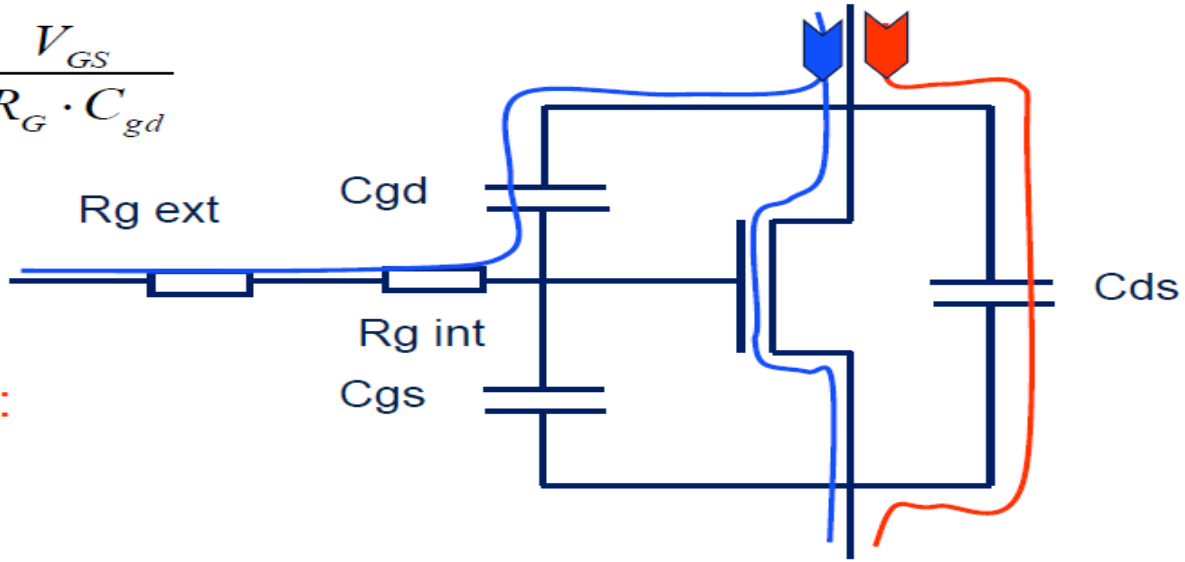
C_{oss}- dominated switching vs. gate control

Gate control:

$$dv/dt = \frac{I_G}{C_{gd}} = \frac{V_{GS}}{R_G \cdot C_{gd}}$$



Coss control:

$$dv/dt = \frac{I_l}{C_{oss}}$$

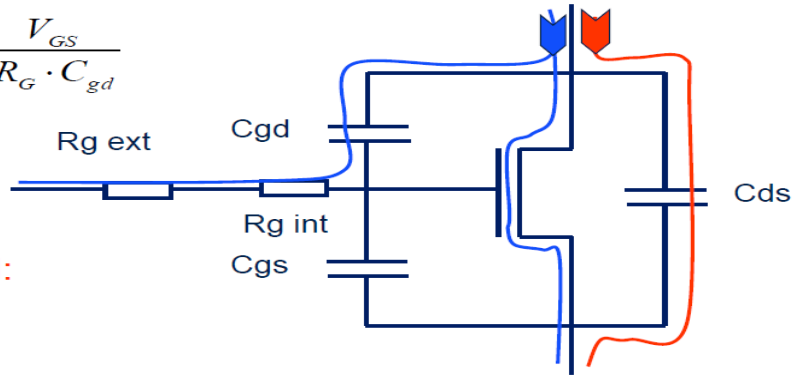
Slowing the switching action of CoolMOS™: Using external Rg

The well-known way to control the switching speed and therefore the EMI behavior is a variation of the external gate resistance. If the resistance will be increased, the time constant determined by this resistance and the capacitance of the MOSFET will be increased as well. The switching transient will be slowed down and thereby the electrical noise becomes lower

Increasing Rg reduce dv/dt

Gate control:

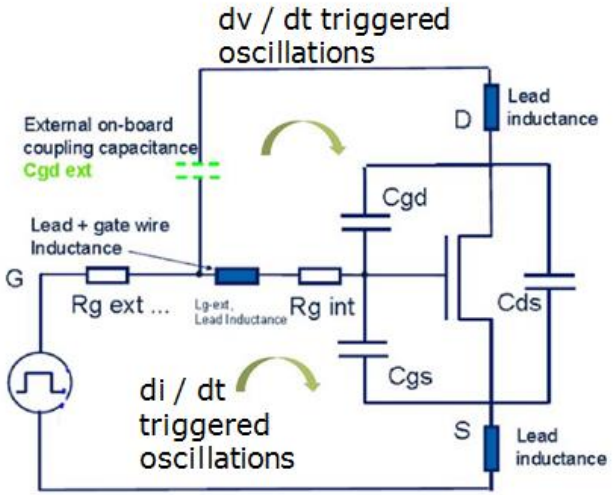
$$dv/dt = \frac{I_G}{C_{gd}} = \frac{V_{GS}}{R_G \cdot C_{gd}}$$



Coss control:

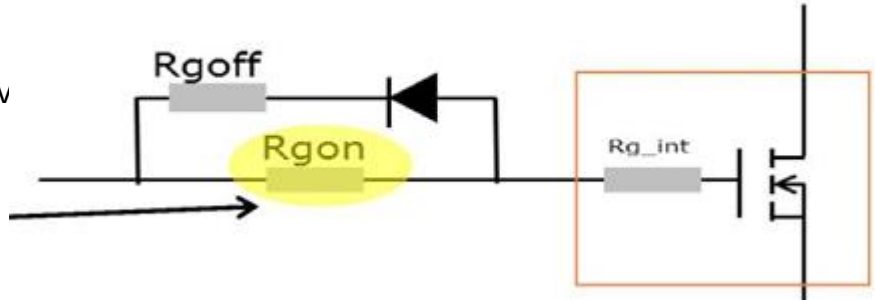
$$dv/dt = \frac{I_l}{C_{oss}}$$

Use of internal and external R_g



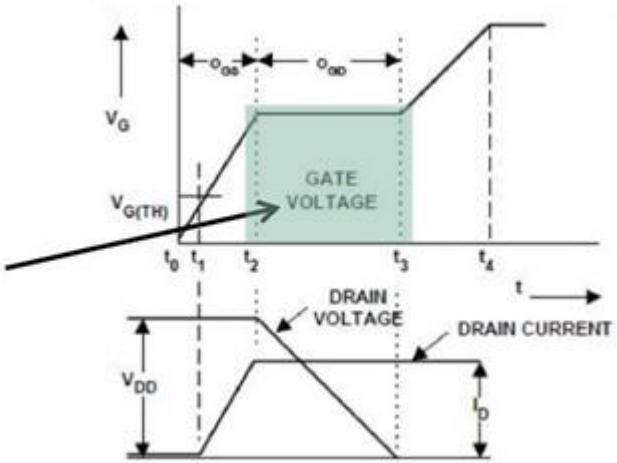
Integrated R_g suppresses oscillations due to dv/dt and di/dt internal to the device

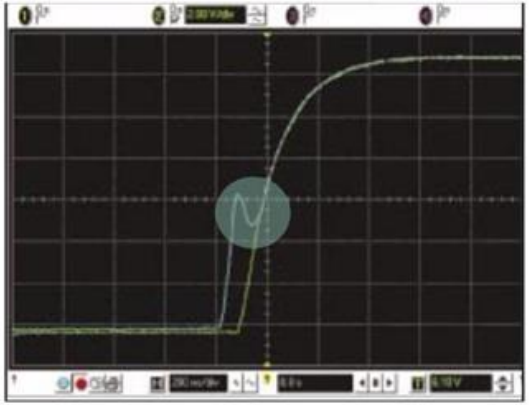
Seperating Rgon and Rgoff helps
> Adjust MOSFET turn-on and turn-off behav individually
> Turn-off resistor impacts efficiency
Turn-on resistor impacts EMI



R_{gon} limits in hard switching power supplies

Miller plateau in hard switched power supply





R_g ↓ Time (ns) in miller plateau ↓ Switching loss

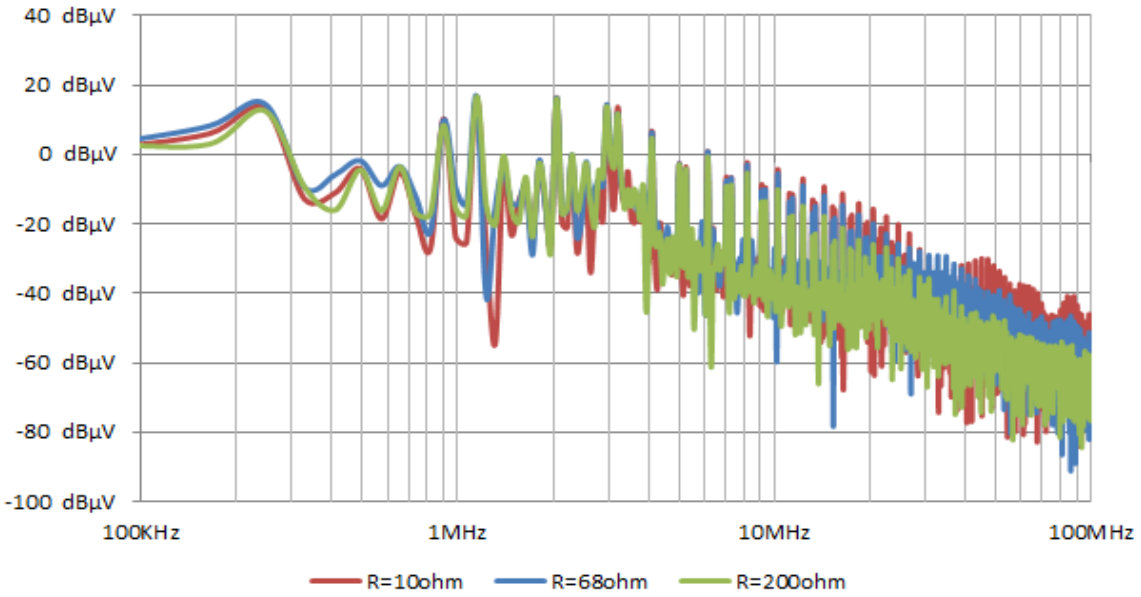
A quasi resonant (QR) flyback power supply has no miller plateau, so R_{gon} value has less impact on efficiency

Time in miller plateau: $t = (R_g * C_{gd} * V_{ds}) / (V_{plateau} - V_{gsth})$

Power loss in miller plateau = $P_{av} * t = 0.5 * V * I_d * t$

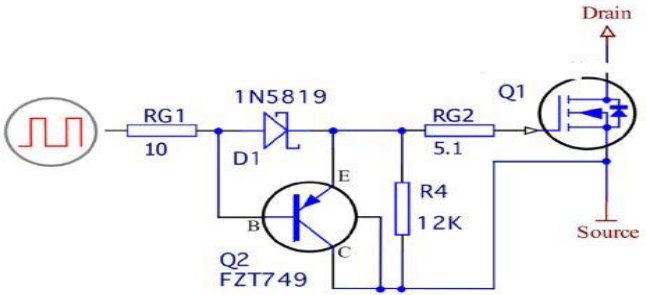
This leads to **lower efficiency** and **higher temperature rise** on the CoolMOS™

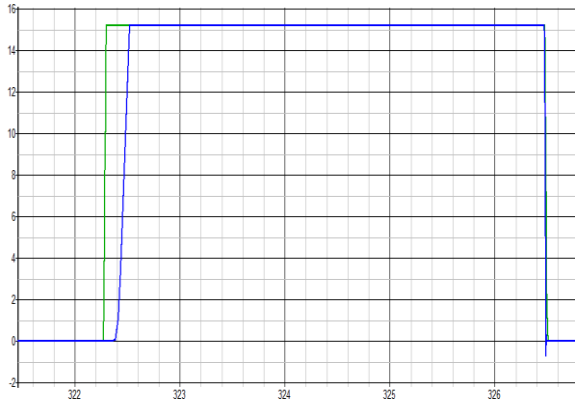
Influence of the external gate resistance



The noise emission can be also controlled in this way in high frequency range

Effect of R_{gon} on EMI signature

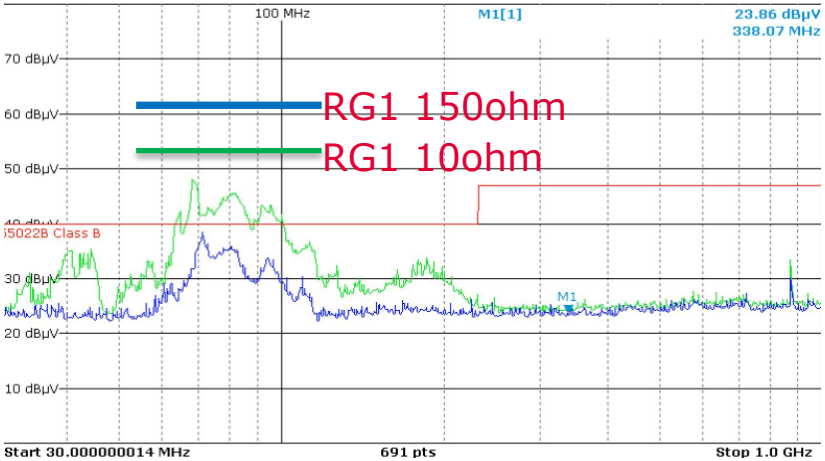




Simulated gate voltage showing reduced slew rate with higher R_g

Increasing external R_g, improves EMI by approx.

5 dBuV in less than 100 Mhz frequency scan range



Simulated radiated emission scan

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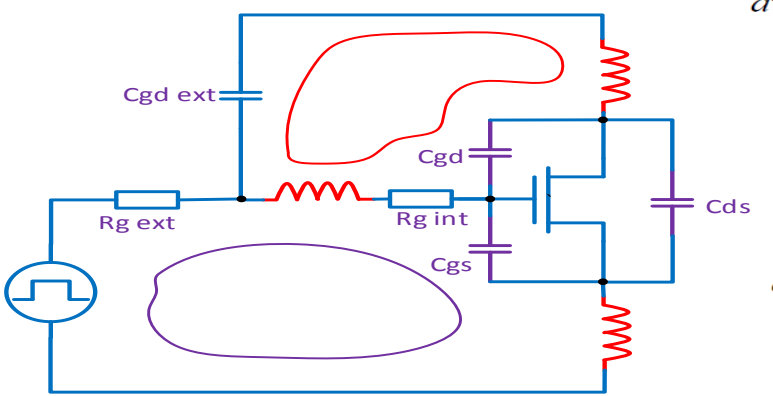
Slowing the switching action of CoolMOSTM: Using external Cgd

Second method to control the switching speed and therefore the EMI behavior is addition of the external gate to drain capacitance. If the capacitance will be increased, the time constant determined by this resistance and the capacitance of the MOSFET will be increased as well. The switching transient will be slowed down and thereby the electrical noise becomes lower.

Increasing Cgd reduces dv/dt

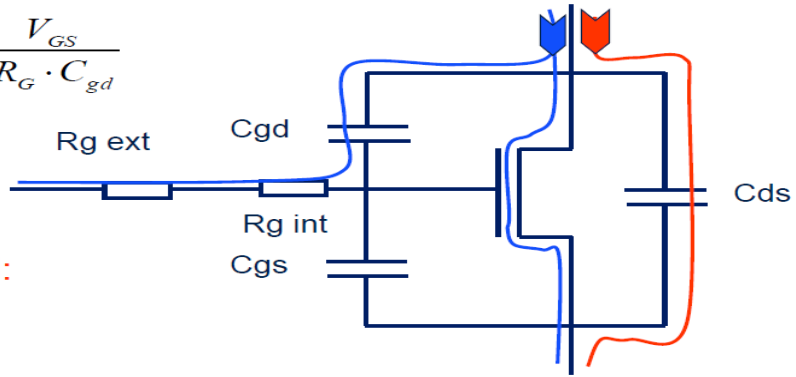


Gate control:

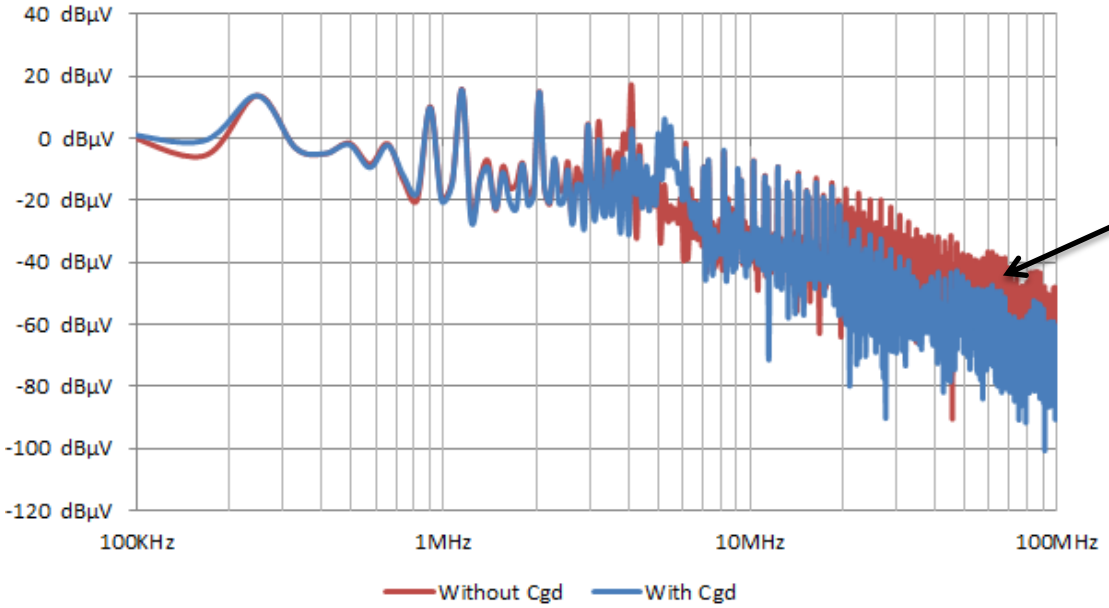
$$dv/dt = \frac{I_G}{C_{gd}} = \frac{V_{GS}}{R_G \cdot C_{gd}}$$

Coss control:

$$dv/dt = \frac{I_l}{C_{oss}}$$



Influence of the external Cgd

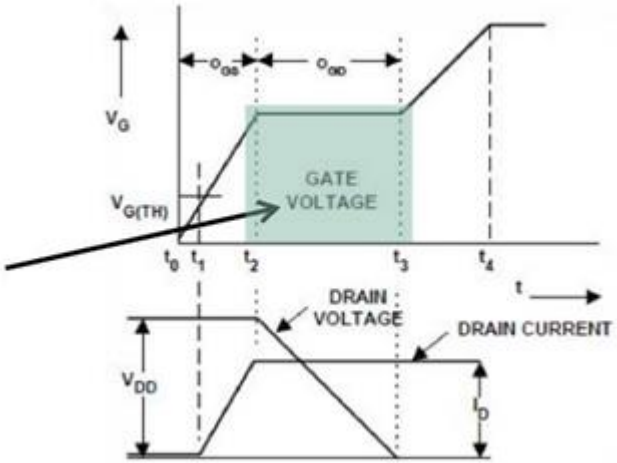


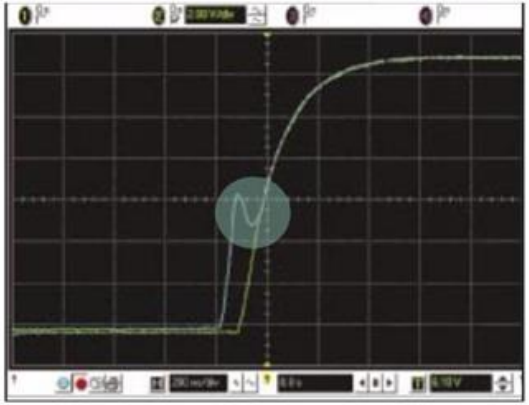
EMI reduced by 10 dBuV in high scan frequency range

Simulated EMI signature

Cgd limits to reduce EMI

Miller plateau in hard switched power supply





C_{gd} ↑ Time (ns) in miller plateau ↑ Switching loss ↑

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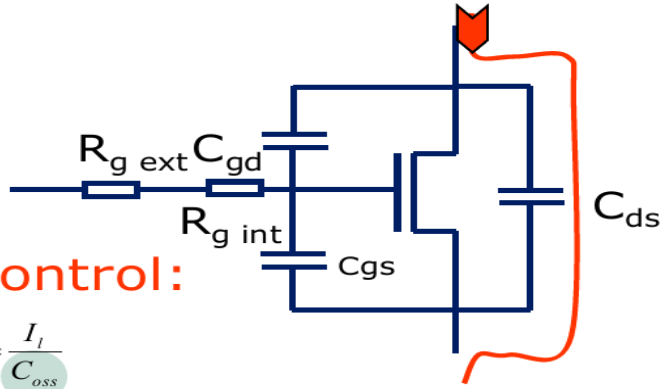
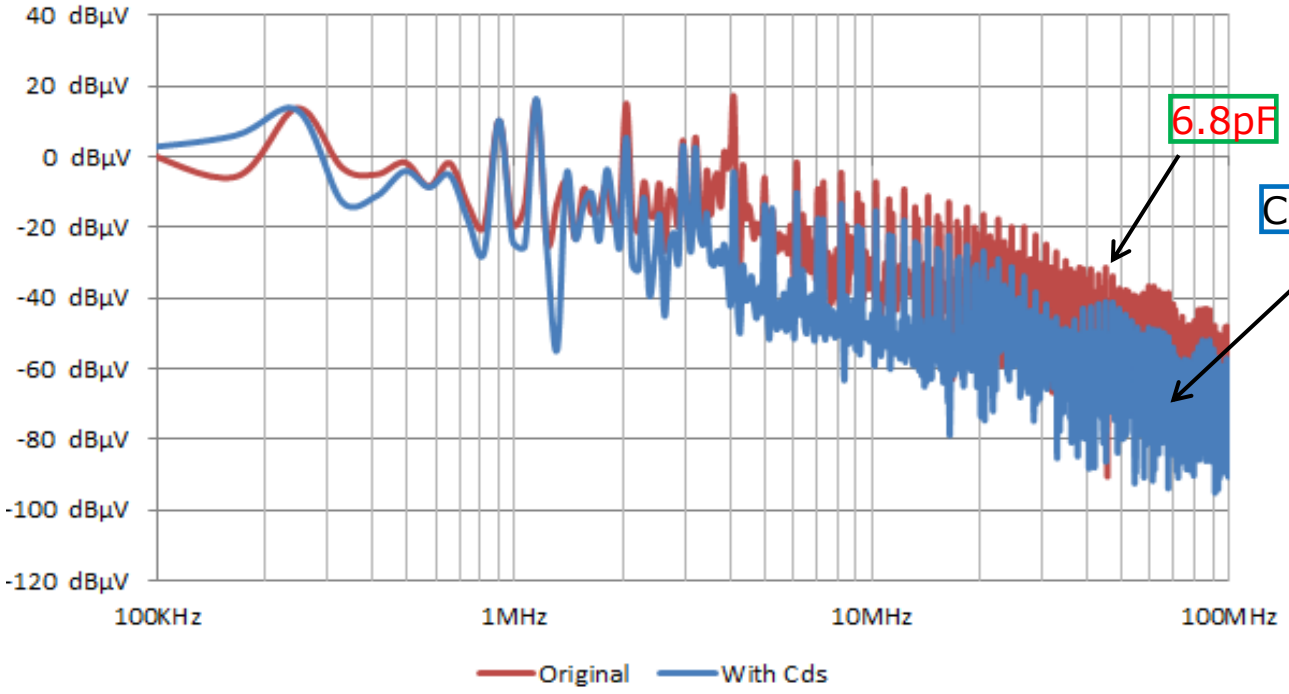
Slowing the switching action of CoolMOS™: Using external Cds

The third way to control the switching speed and therefore the EMI behavior is increasing the output capacitance of the MOSFET. If the capacitance will be increased in a Coss dependent switching like in the QR flyback, the switching transient will be slowed down and thereby the electrical noise becomes lower.

Increasing C_{ds} / C_{oss} reduces dv/dt



Influence of the external Cds



EMI reduced by 10 dBuV across scan frequency range

Simulated EMI signature

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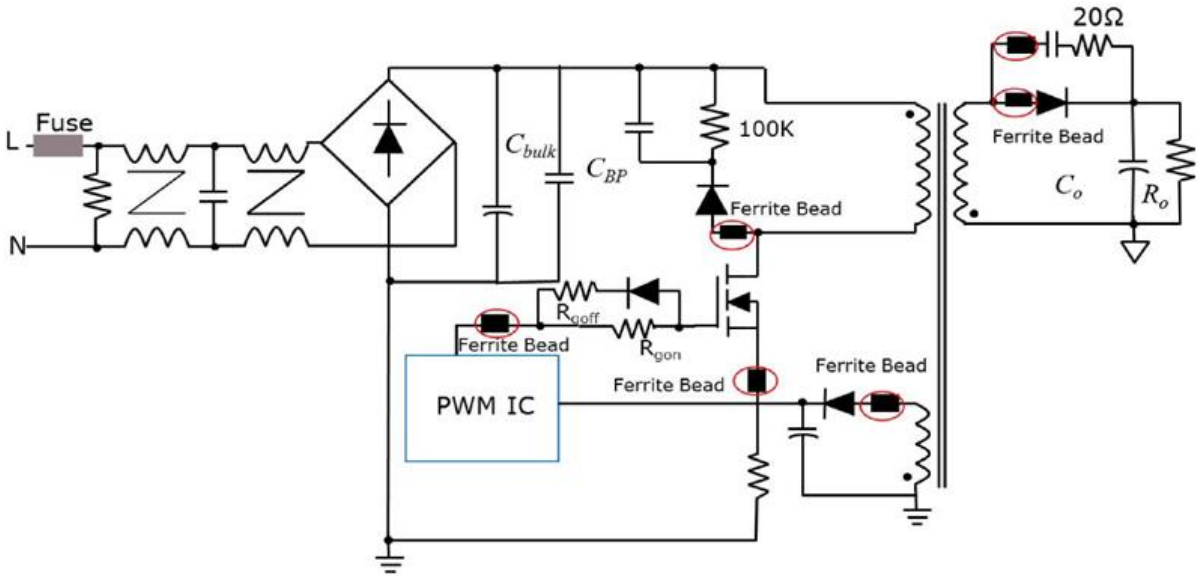
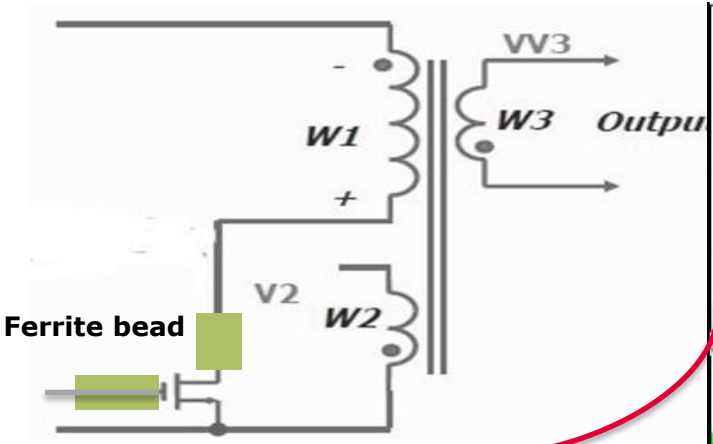
Placing ferrite beads around CoolMOS™

di/ dt = V / L, where V is the oscillation (noise) voltage and L is the stray inductance



Use ferrite bead to reduce FET di/dt

Use of Ferrite bead to Suppression EMI(15W)



with Ferrite bead			without Ferrite bead		
V_in	I_out	Eff	V_in	I_out	Eff
90.01	0.4981	80.831	90.01	0.4981	80.841
90	0.8749	83.61971	90	0.8749	83.60971
90.01	1.2504	84.63238	90.01	1.2504	84.61238
90.01	1.6251	85.679	90.01	1.6251	85.66
90.01	1.9998	86.25454	90.01	1.9998	86.252
264.16	0.4983	86.8961	264.16	0.4983	86.8961
264.15	0.8748	87.8801	264.15	0.8748	87.8801
264.16	1.2502	88.01185	264.16	1.2502	88.02
264.16	1.625	87.62	264.16	1.625	87.6
264.15	1.9997	87.01646	264.15	1.9997	87.1

No significant efficiency difference can be seen by adding ferrite bead

Without Ferrite bead

With Ferrite bead

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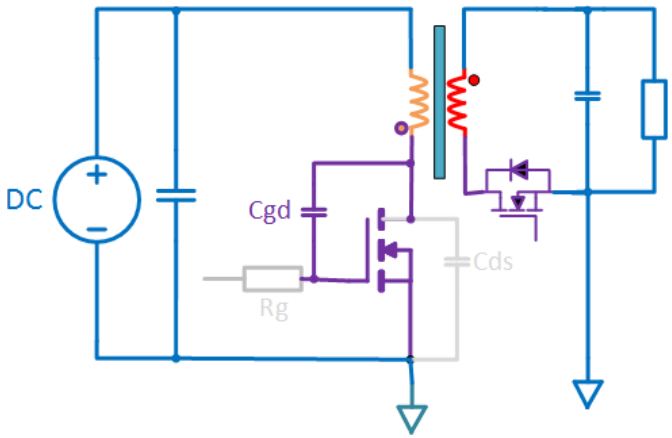
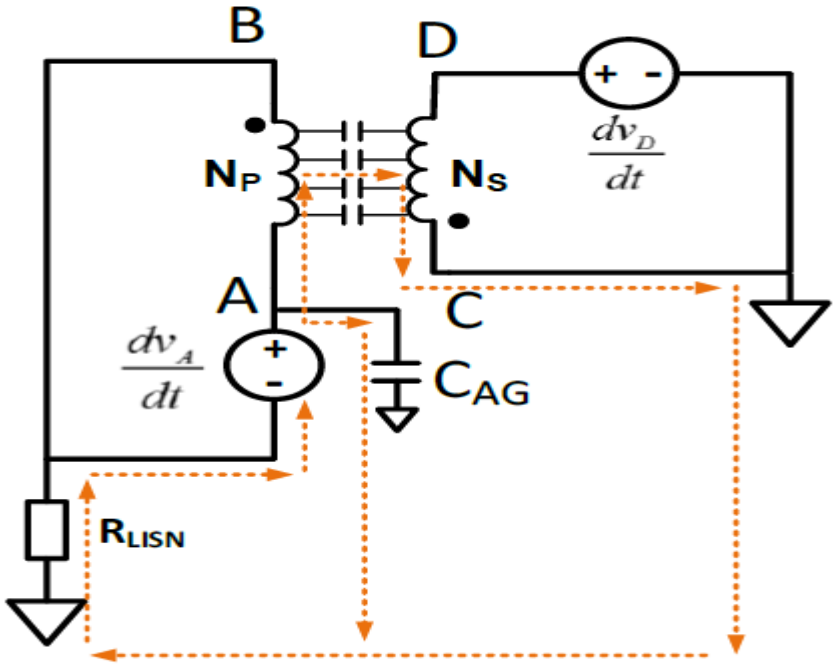
Flyback电路变压器共模噪声抵消技术

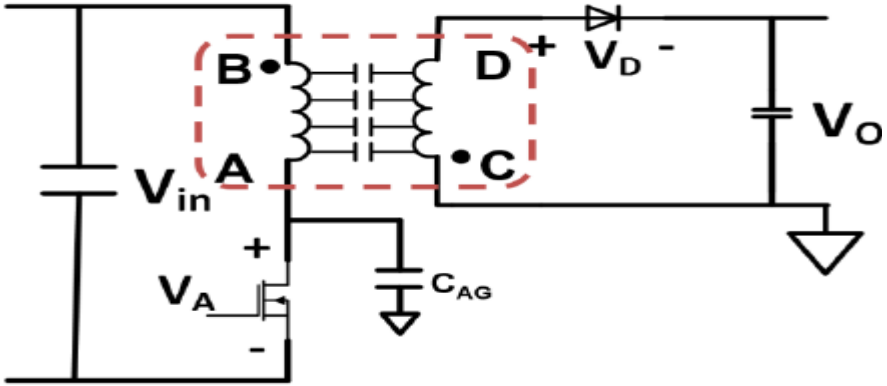


反激变换器拓扑

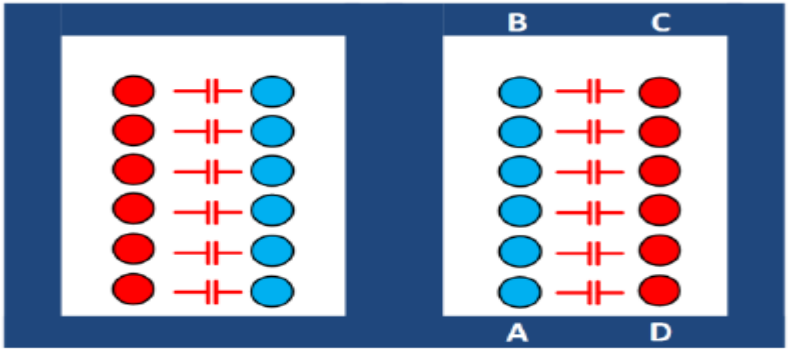


反激变换器的共模噪声传播路径

Flyback电路变压器共模噪声抵消技术

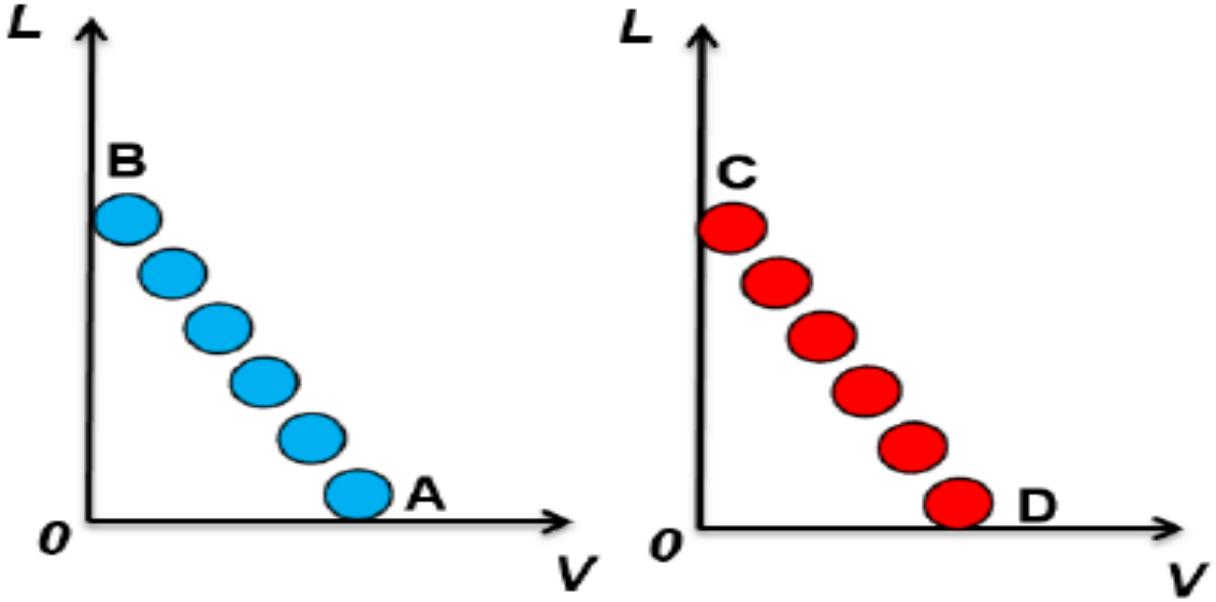


反激电路拓扑



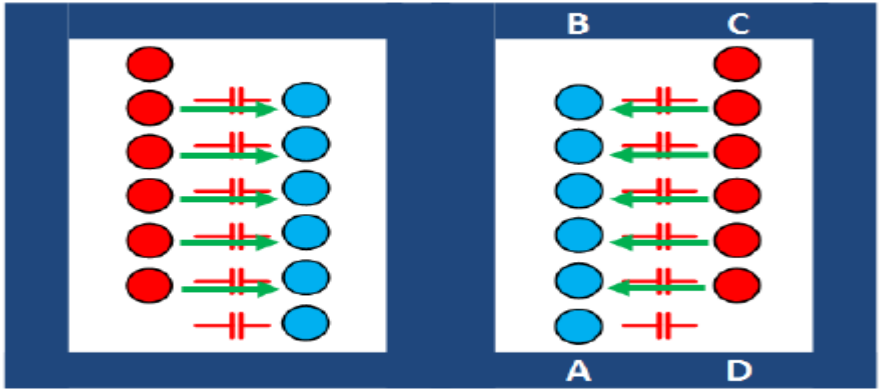
1：1变压器结构图

Flyback电路变压器共模噪声抵消技术

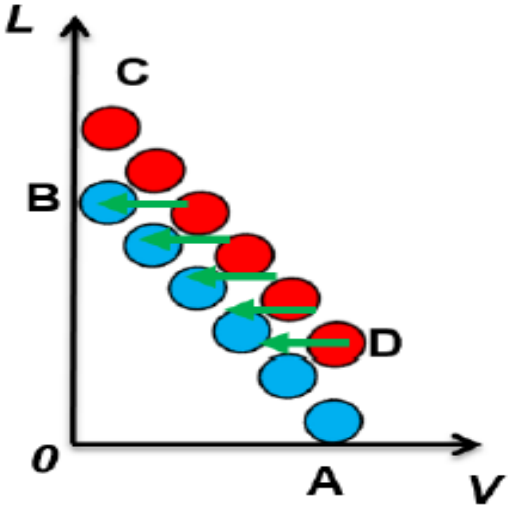


初级绕组和次级绕组的电压分布

Flyback电路变压器共模噪声抵消技术

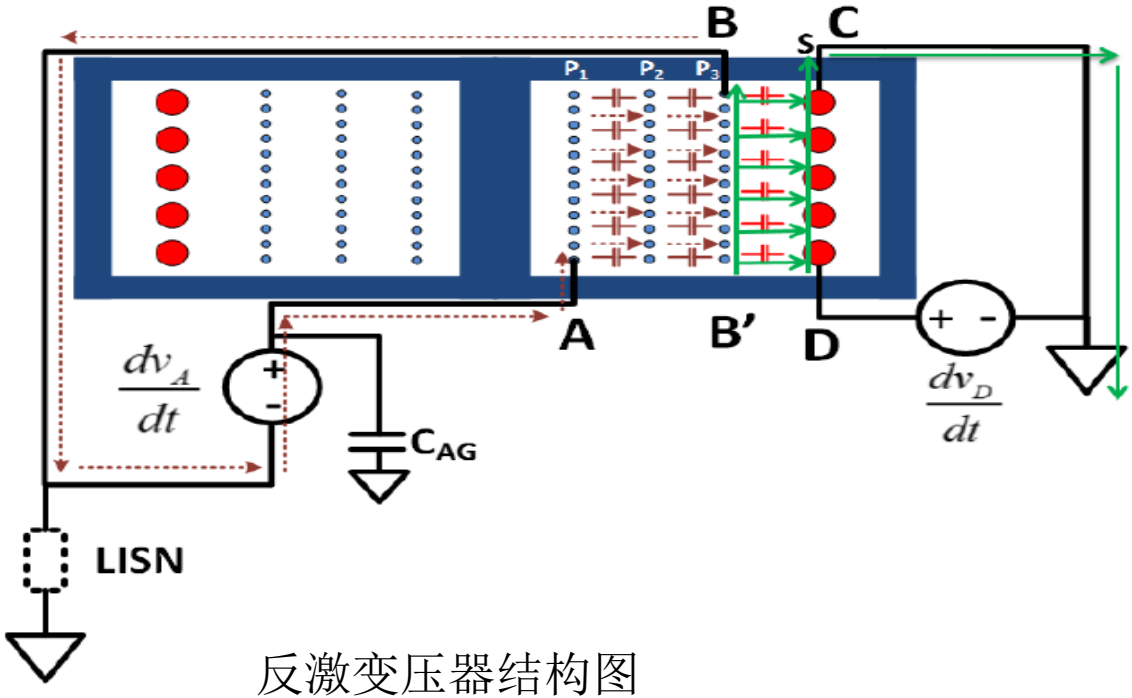


当线组不重合时



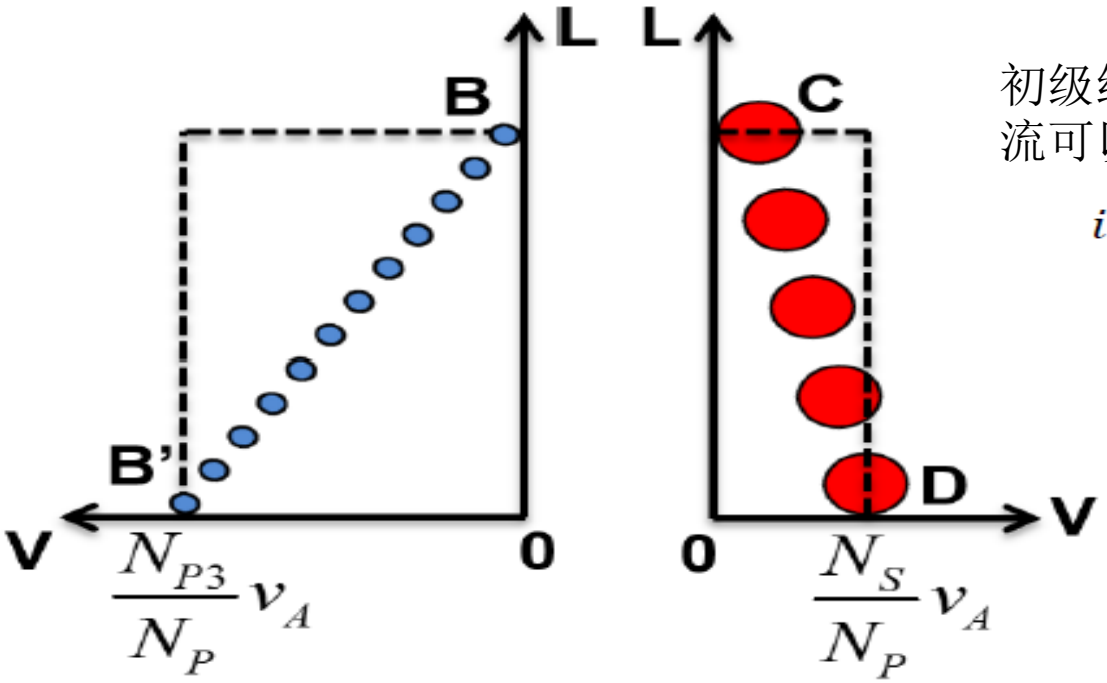
初级绕组和次级绕组的电压分布

Flyback电路变压器共模噪声抵消技术



反激变压器结构图

Flyback电路变压器共模噪声抵消技术

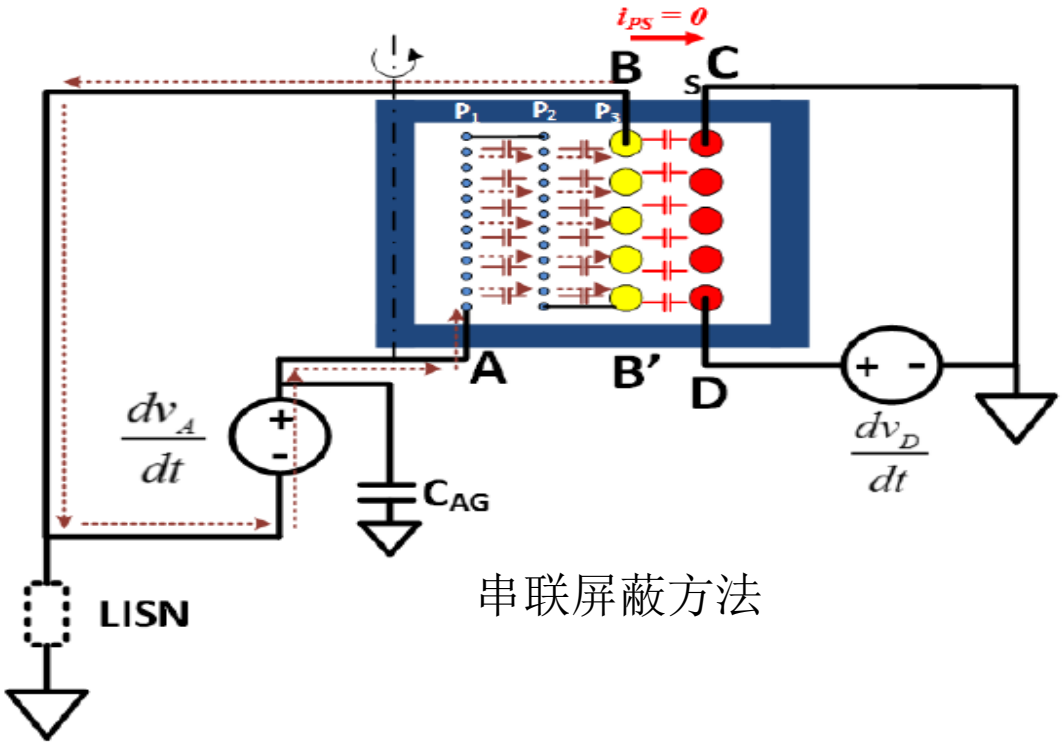


初级线组到次级绕组的总位移电流可以计算出：

$$i = C_{PS} \frac{d}{dt} \frac{v_A}{2N_P} (N_{P3} - N_S)$$

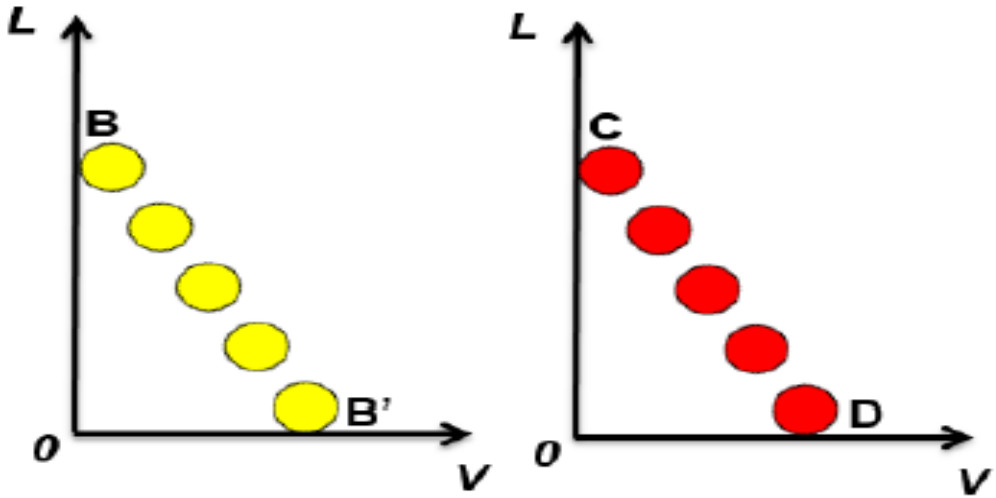
初级P3绕组和次级绕组的电压分布

Flyback电路变压器共模噪声抵消技术



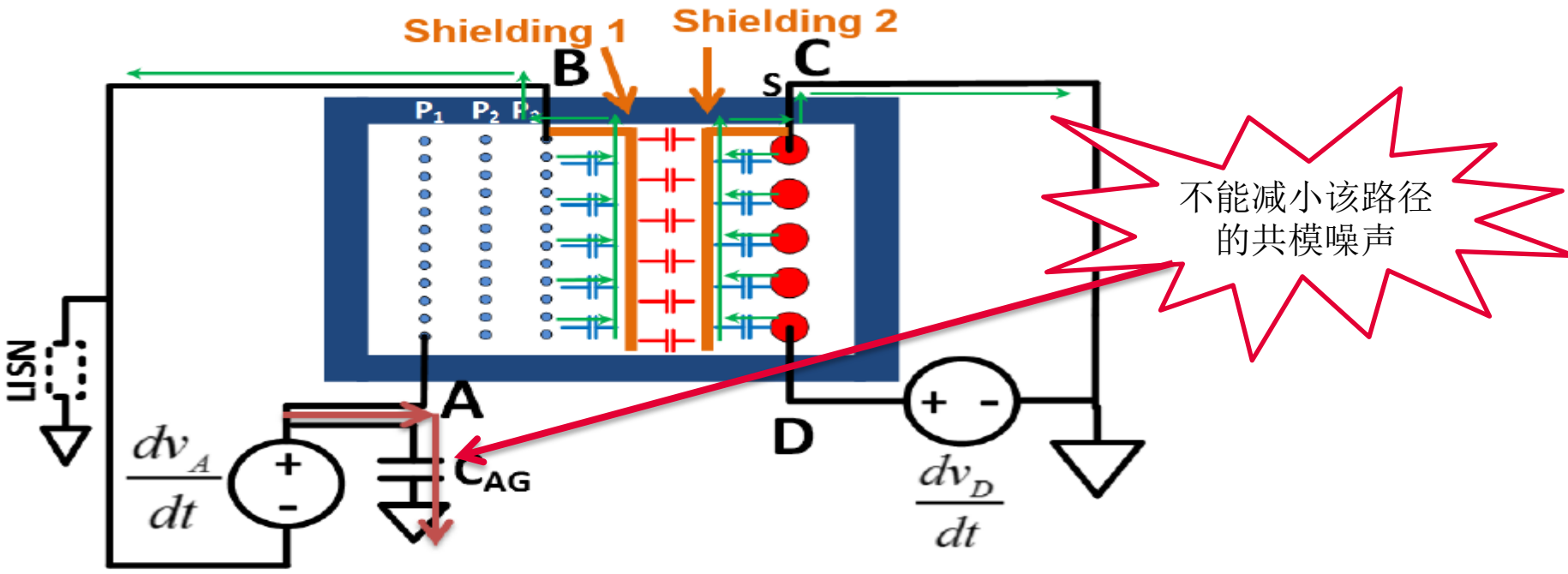
串联屏蔽方法

初级P3绕组和次级绕组的电压分布



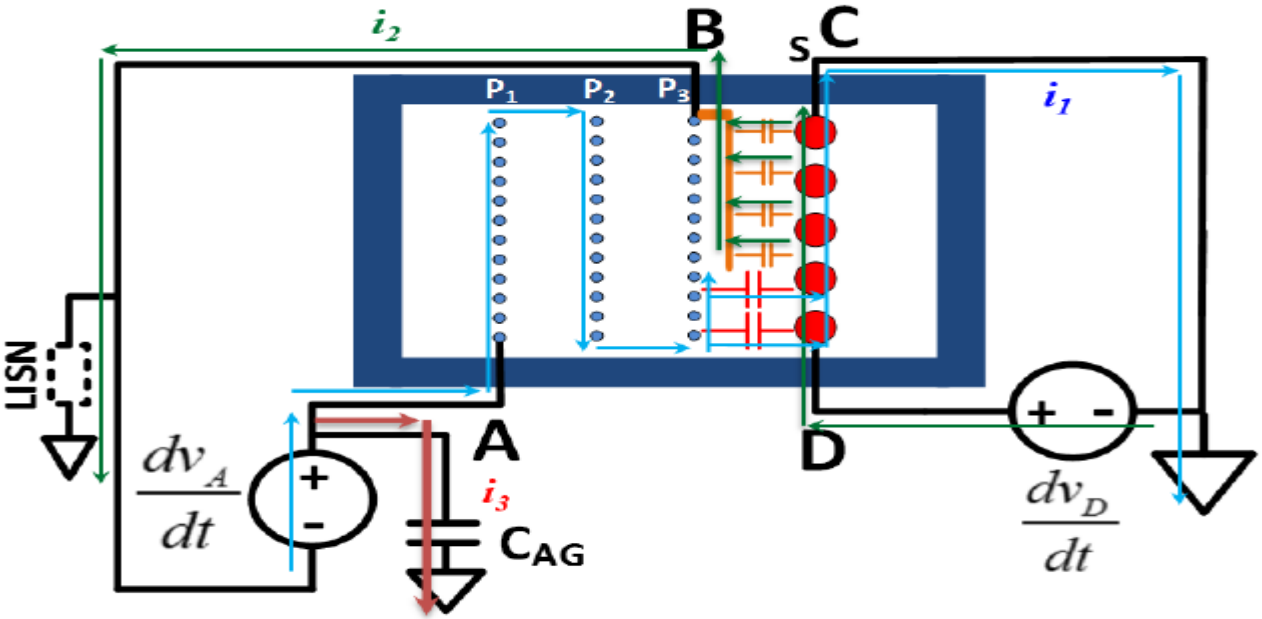
初级P3绕组和次级绕组的电压分布

两层屏蔽方法



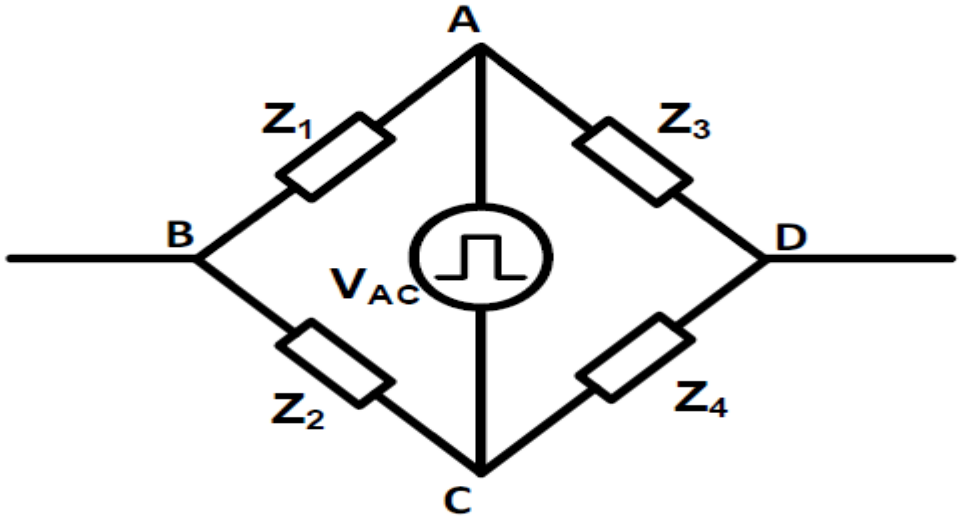
两层屏蔽方法

部分屏蔽



$$i_1 + i_2 + i_3 = 0$$

惠斯登电桥结构

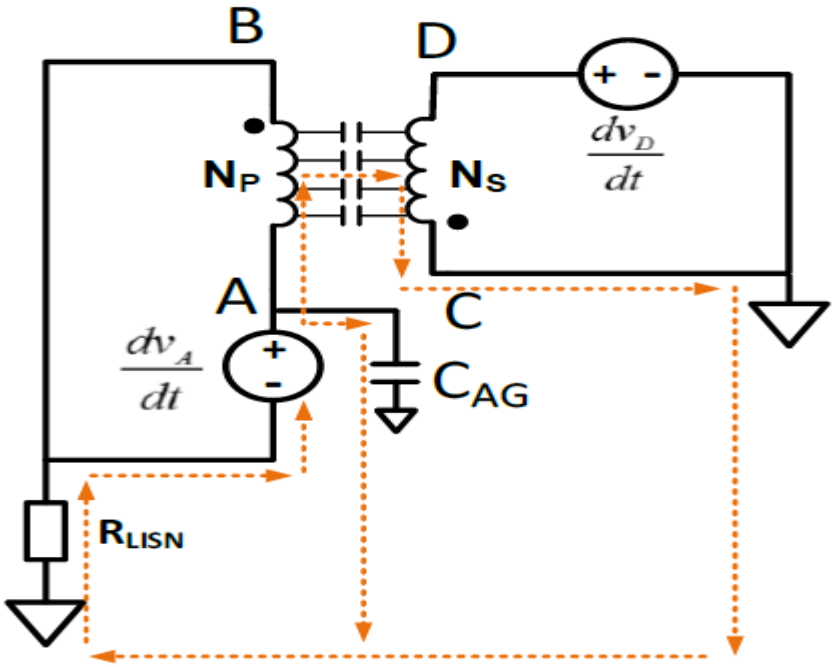


惠斯登电桥结构

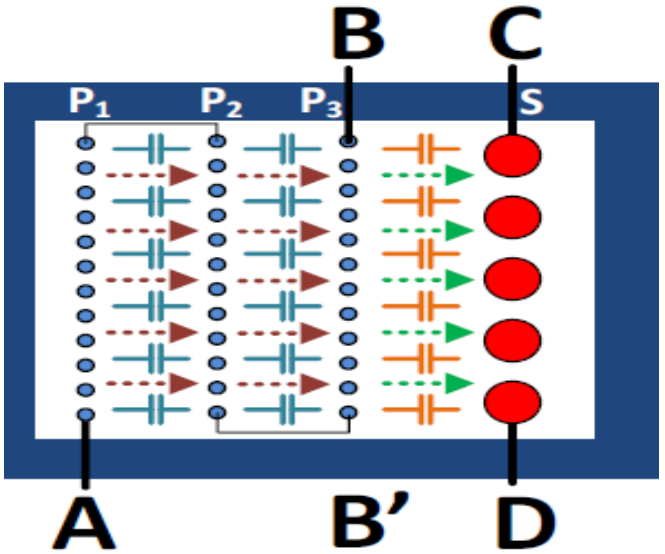
当Z1/Z2=Z3/Z4 电桥平衡，B点与D点电压一样因此没有电流流过。

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4}$$

变压器共模噪声抵消技术

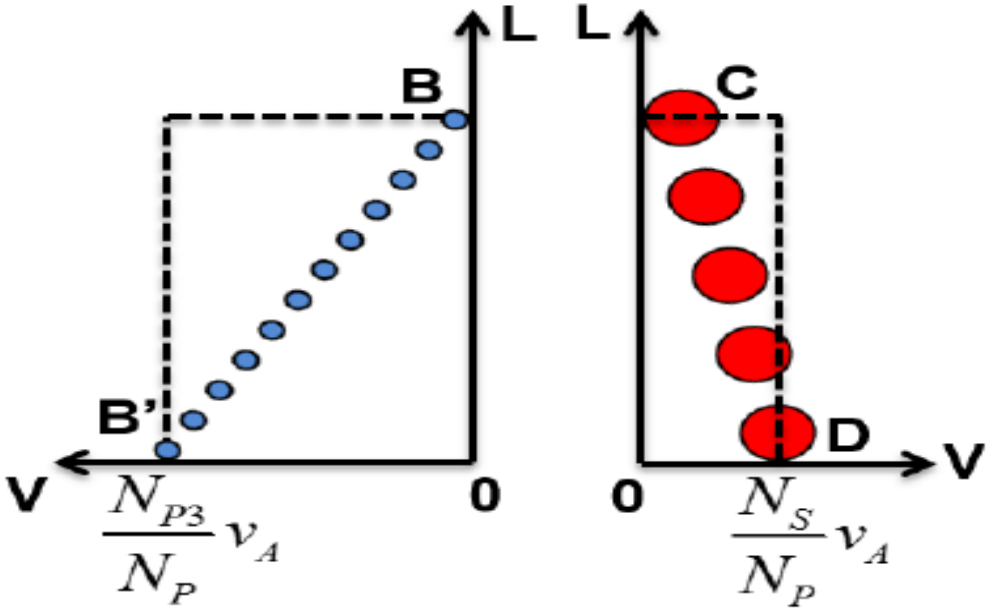


使用电压源取代MOSFET



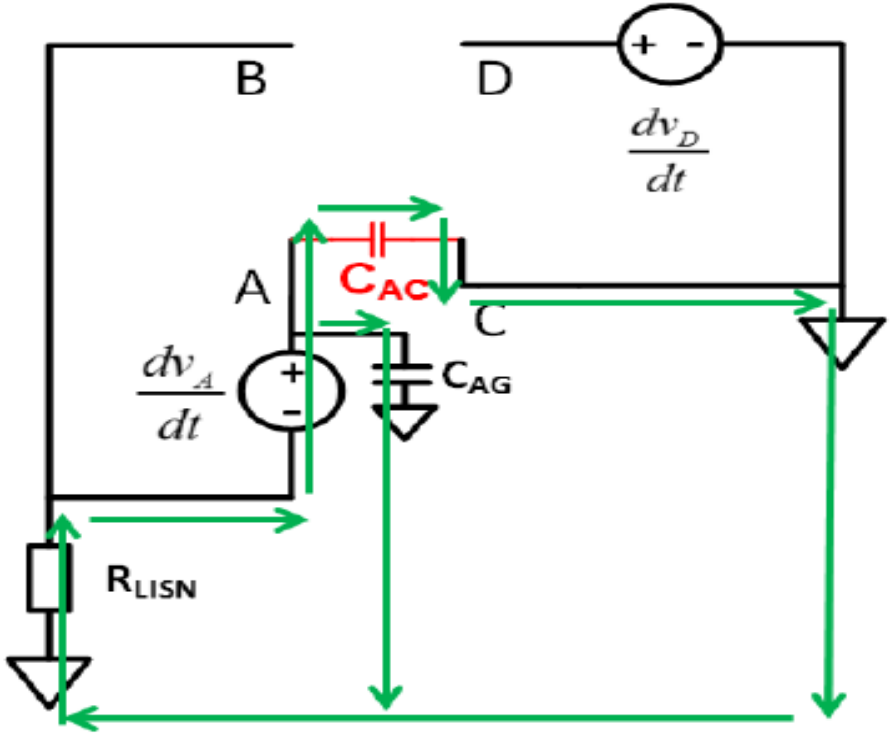
变压器结构

绕组电压分布



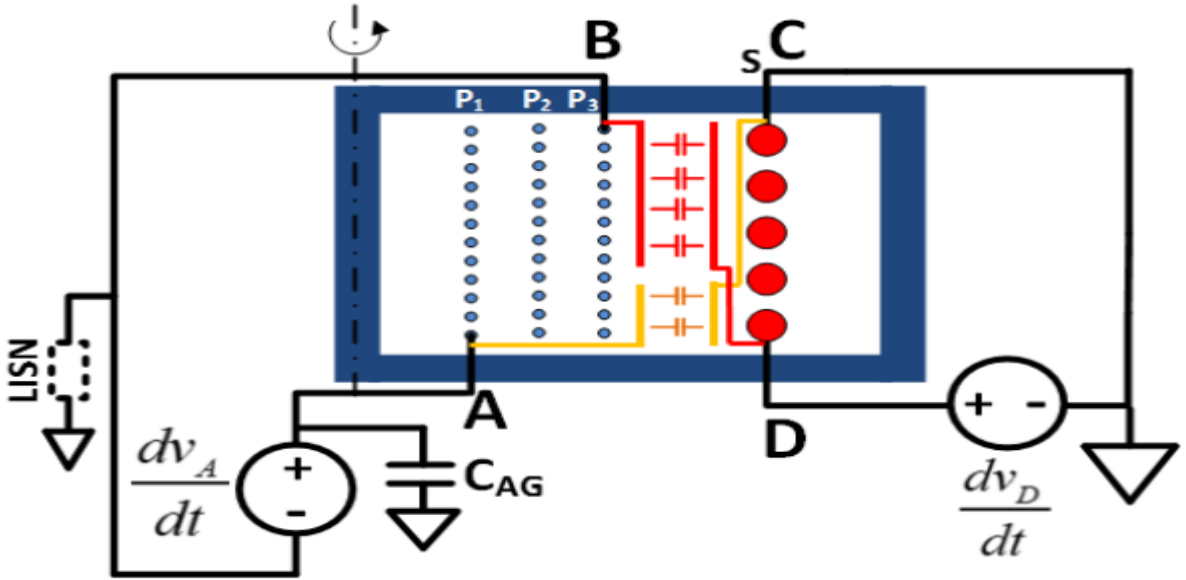
$$i = C_{PS} \frac{d}{dt} \frac{v_A}{2N_P} (N_{P3} - N_S)$$

变压器共模噪声抵消技术

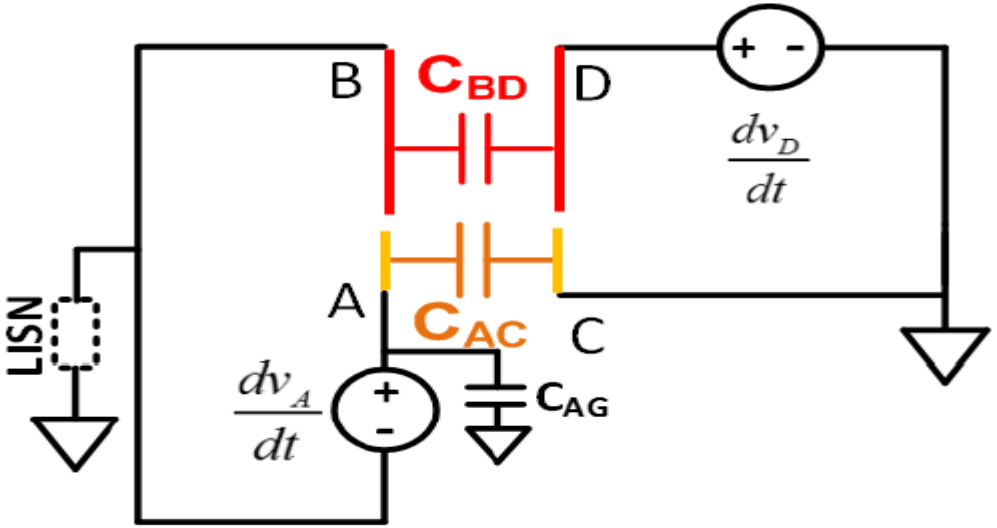


反激变换器的共模噪声

Flyback电路变压器共模噪声平衡方法

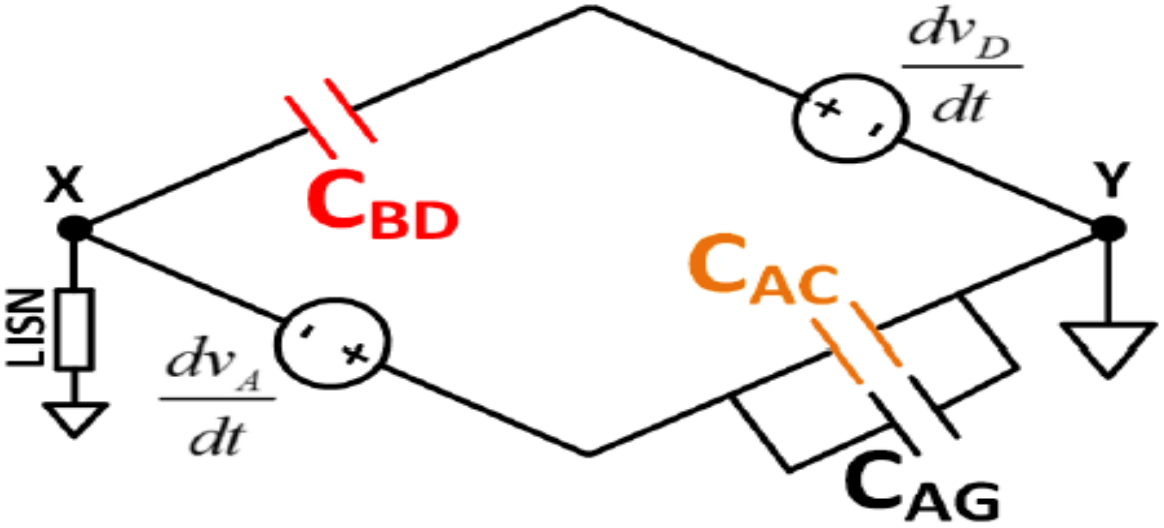


Flyback电路变压器共模噪声抵消技术的共模噪声模型



使用双屏蔽平衡技巧的反激变换器共模噪声模型

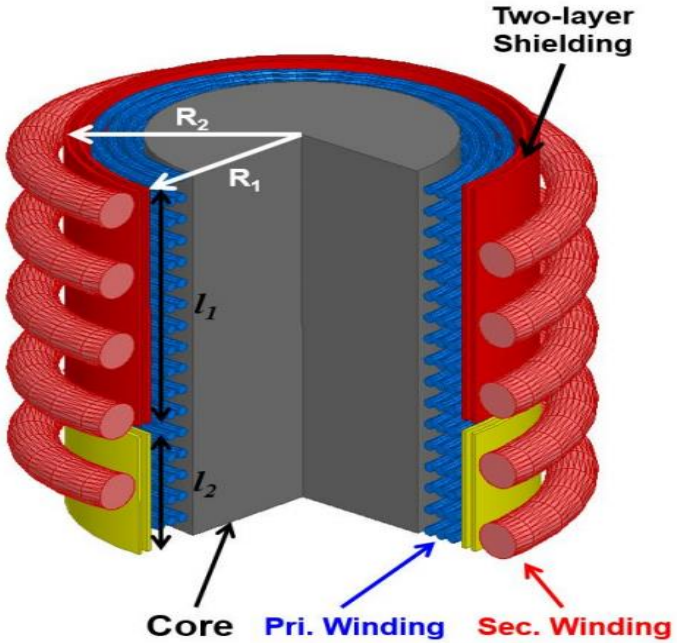
桥式电路的CM模型



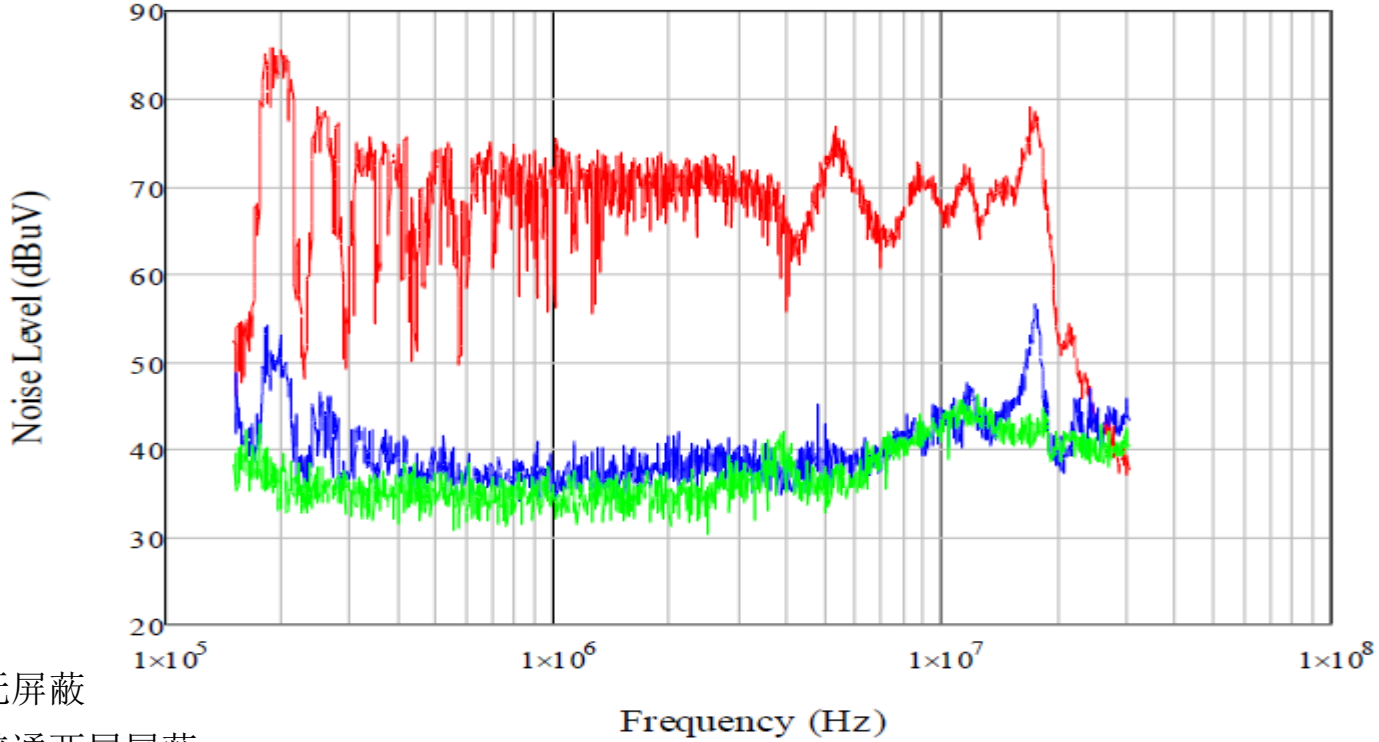
桥式电路的CM模型

$$\frac{dv_A/dt}{dv_D/dt} = \frac{C_{BD}}{C_{AC}+C_{AG}}$$

变压器3D图



实测EMI对比图

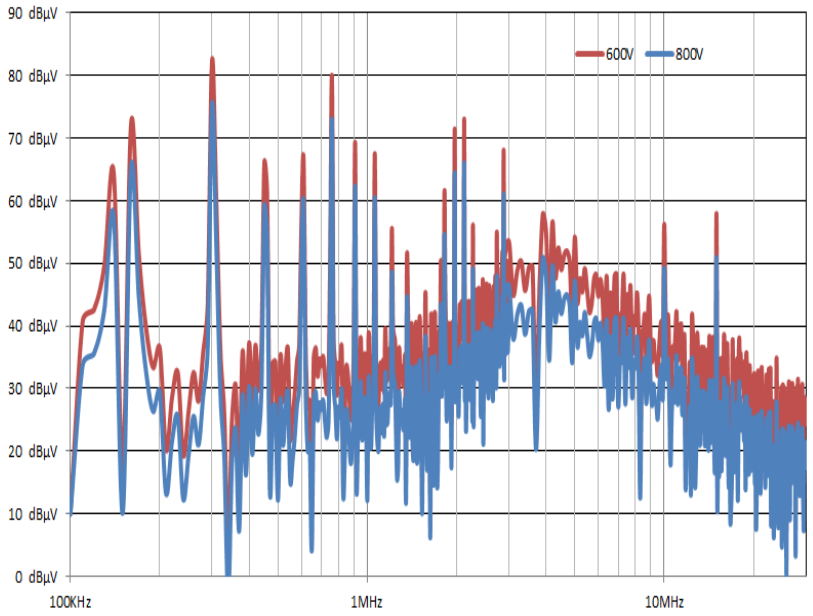


无屏蔽

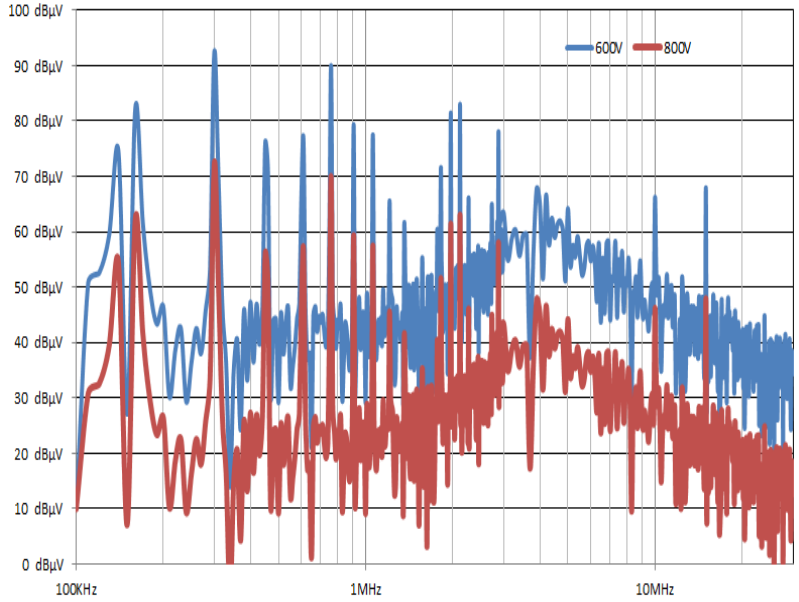
普通两层屏蔽

平衡屏蔽法

反射电压对反激电路EMI的影响



图A 漏源极电压的频谱比较



图B 漏源极电流的频谱比较

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